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Self-patterning of high-performance thin film transistors

Kuo-Jui Chang [b], Feng-Yu Yang [a,*], Cheng-Chin Liu [b], Meei-Yu Hsu [a], Ta-Chuan Liao [b], Huang-Chung Cheng [b]

[a] Materials and Chemical Laboratories, Industrial Technology Research Institute, 195, Sec. 4, Chung Hsing Road, Chutung, Hsinchu 310, Taiwan
[b] Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan

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ABSTRACT

We have developed a technique for the preparation of thin film transistors (TFTs) through the self-patterning of various organic and inorganic materials via solution processing using a wide range of solvents. To obtain selectively self-patterned layers, we treated the oxide dielectric with two-phase patterned self-assembled monolayers of hexamethyldisilazane (HMDS) and octyltrichlorosilane. The conducting polymer poly(3,4-ethylenedioxythiophene) doped with poly(styrene sulfonic acid) in water and the dielectric polymer poly(vinyl phenol) in propylene glycol methyl ether acetate were both selectively deposited and patterned on the HMDS regions with high-quality feature shapes. When source and drain electrodes were patterned on the bottom-gate oxide wafer, we also self-patterned organic and inorganic semiconductors around the channel (HMDS) regions. These TFT devices exhibited moderate to good electronic characteristics. This method has great potential for the economical full solution processing of large-area electronic devices. The selectivity in the patterning phenomena can be understood in terms of surface energy interactions.

1. Introduction

Organic thin film transistors (OTFTs) are attracting much attention for their potential applications in next-generation devices, such as flexible displays, RFIDs, smart cards, electronic paper, sensor arrays, and low-cost disposable electronic devices [1–6]. They exhibit several advantageous features – large areas, low cost, light weight, mechanical flexible, and low-fabricating temperature – that make them preferable to inorganic-based devices; in addition, they can be prepared directly on flexible plastic substrates. During the last two decades, a number of remarkable improvements – in materials development [7–9], the modification of self-assembly monolayers (SAMs) at organic semiconductor–dielectric interfaces [10–13], and device structure engineering [14–16] – have made OTFTs competitive with silicon-based devices. For practical applications, efficient patterning is crucial to the development of electronic devices and circuits. Notably, semiconductors that are not patterned exhibit cross-talk between adjacent devices, parasitic resistance, and gate leakage current (I_G) and drain current (I_D) offsets that are more dramatic than those of patterned systems [17,18]. There are two major approaches that are used to deposit the active semiconductor layer: thermal evaporation and solution processing. Although thermal evaporation through a shadow mask can produce well-ordered patterned films, the throughput is slow and involves expensive vacuum systems. Low-cost solution processing, on the other hand, usually produces non-patterned films that cover the entire substrate. When patterning semiconductor films, which are usually sensitive to oxygen, water, and solvents, common photolithography methods cannot usually be applied directly without a protective capping layer present on top of the semiconductor layer prior to coating of the photoresist. Parylene-C and polyvinylalcohol (PVA) [19–21] and their organic/inorganic bilayers of SiO_2, SiN_x, Al_2O_3, and Al [22] are the most common materials used as protecting layers. Several patterning methods have been developed recently for use in conjunction with solution

* Corresponding author. Tel.: +886 3 5912643; fax: +886 3 5827694.
E-mail address: FengYuYang@itri.org.tw (F.-Y. Yang).

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processing, including ink-jet printing, screen printing [23], soft lithography [24,25], laser-assisted patterning [26,27], contact printing [28], and self-organization processes [29–33]. Among these methods, self-organization has great potential for use in the fabrication of high-throughput, low-cost electronics without degrading their OTFT performances. For example, Bao et al. [29] reported a microcontact printing (μCP) method for transferring low-molecular-weight siloxane oligomers from PDMS stamps to pattern organic poly(3-hexylthiophene) (P3HT) and poly(vinyl phenol) (PVP) materials via selective wetting/dewetting to fabricate regions with and without oligomers [29]; nevertheless, the interface of the channel region was only the bare surface, lacking a modification layer. Many authors have determined that modification layers present between the dielectric and organic active material are necessary to improve the interfacial adhesion and the film's crystallinity, thereby providing more-stable devices exhibiting higher carrier mobilities [10]. During the preparation of this manuscript, two research groups published self-organization processes featuring the treatment of two modification layers on silicon oxide surfaces [32,33]. Minari et al. [32] reported a surface presenting phenyl-terminated SAMs as channel regions and hexamethyldisilazane (HMDS) units covering the rest of the surface. Small organic molecules that had been drop-cast from toluene solutions were selectively crystallized on the phenyl-presenting SAM regions. Kim et al. [33] coated a hydrophobic fluoropolymer film onto silicon dioxide and then modified the channel regions with HMDS. A soluble pentacene derivative was then self-deposited from a xylene solution onto the channel areas. Although these two initial studies [32,33] appear to have several advantages over simple mono-modification treatment [29–31] the authors studied the patterning of semiconductors in nonpolar solvents only; they did not explore the use of other materials (e.g., conducting polymers, organic gate dielectrics) or other polar and nonpolar solvents. In addition, the origins of the self-organization processes were considered to occur mostly through differences in the water contact angles of the substrates inducing the hydrophilic/hydrophobic properties; there remains much room to provide a more appropriate explanation of these phenomena.

In this study, we developed a new system for the self-patterning of two types of SAMs on silicon dioxide surfaces, with HMDS forming channel regions and octyltrichlorosilane (OTS) covering the remaining areas. We prepared these patterns readily using traditional photolithography processes. In addition to investigating several organic and inorganic semiconductors, we also processed the conducting polymers from aqueous solutions and employed organic gate dielectric materials. We explain the self-patterning phenomena in terms of surface energy differences – rather than the previously reported simple hydrophilic/hydrophobic water contact angle theory.

2. Experimental section

Materials: PVP (M_w = 20,000), PMF (M_w = 511), OTS, HMDS, chlorobenzene, toluene, propylene glycol monomethyl ether acetate (PGMEA), CH_2Cl_2, hexane, and acetone were purchased from Sigma–Aldrich and used without further purification. Regioregular P3HT was purchased from Aldrich and purified through Soxhlet extractions with hexane and CH_2Cl_2 to remove low-molecular-weight chains. 13,6-*N*-sulfinylacetamidopentacene (NSFAAP) and zinc acetate were also obtained commercially from Aldrich and used directly. Poly(9,9-dioctylfluorene-*alt*-bithiophene (F8T2) was purchased from American Dye Source. The PEDOT:PSS water solution (AI4083) was purchased from Bayer.

Device fabrication: We prepared the substrate using the self-patterning process presented in Fig. 1. We employed a silicon wafer presenting thermally grown SiO_2 (d = 100 nm) as the substrate. The source and drain (S/D) Pt/Ti (50 nm/2 nm) electrodes having channel widths and lengths of 1000 and 10 μm, respectively, were prepared using a photolithography/Pt–Ti deposition/lift-off (acetone) process. The entire device surface was treated with HMDS vapor and then cured at 150 °C for 0.5 h, and then the channel regions of the device were covered with photoresist using conventional photolithography processing. The remaining region not covered with the photoresist was treated through O_2 plasma bombardment and then treated with OTS vapor then cured at 100 °C for 0.5 h. Finally, the photoresist was removed to provide a substrate presenting HMDS in the channel regions and OTS over the remaining areas.

Electrical Measurements: All TFT devices arrays in this study, each containing 20 devices were fabricated. To ensure accuracy of data that were collected, we measured at least 10 devices for each array and no significant (<10%) variations were observed from device to device. All *I*–*V* measurements of our OTFT devices were recorded at room temperature under ambient conditions using an Agilent 4156C semiconductor parameter analyzer. The thicknesses of the corresponding films were determined through cross-sectional scanning electron microscopy (SEM). The surface energies of the various SAM surfaces were determined through contact angle measurements using a FACE contact-angle meter (Kyowa Kaimenkagaku Co.) and distilled water and CH_2I_2 as probe liquids.

3. Results and discussion

We employed various solutions of organic and inorganic materials to examine the scope of this self-patterning method; Fig. 2 presents their chemical structures. After depositing a drop of the semiconductor solution [P3HT (5 mg) in dichlorobenzene (1 mL)] onto the HMDS/OTS-presenting S/D electrode-patterned substrate and then decanting the substrate to remove the large droplet, we found that some small droplets remained adhered to the HMDS regions. After the solvent had dried, the resulting films were isolated with finely featured shapes on the HMDS region. Thus, using this approach, we fabricated a bottom gate, bottom contact configuration of the patterned P3HT-OTFT. Fig. 3a displays an optical micrograph of the with uniformly patterned P3HT-OTFT device array. A magnified image of the P3HT-OTFT single device (Fig. 3b)