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A novel majority based imprecise 4:2 compressor with respect to the current and future VLSI industry

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ABSTRACT

Imprecising the arithmetic hardware blocks is well known as one of the brilliant approaches that increase the performance of digital signal processors (DSP) at the cost of imposing some acceptable errors. Making a trade-off between the performance and the enormous results of a given system is a challenge which has attracted the interest of many researchers in recent years. In this paper, we focus on the design of an imprecise 4:2 compressor which lies at the heart of inexact multipliers. The proposed imprecise 4:2 compressor by utilizing only one majority gate brings significant efficiency in implementation of today's technologies like FinFET and future majority based emerging technologies such as QCA. The evaluation results in both of aforesaid technologies demonstrate the remarkable improvement of the proposed design compared to related works. In addition, employing the proposed imprecise 4:2 compressor in an image processing application confirms the qualitative acceptability of the proposed design.

1. Introduction

High accuracy and reliability are important features in the semiconductor industry which are involved in designing computing structures beside efficiency in performance and power consumption [1]. Embedded digital arithmetic blocks in these devices are also not excluded from the above-mentioned facts [2]. Nonetheless, many applications can sustain errors and non-accurate computation and yet the results are good enough to use. Multimedia applications like image processing are examples of a suitable case to utilize imprecise algorithms and structures [3]. During recent decades, the market of electronic portable devices has witnessed tremendous growth [4]. In portable devices, the source of energy is provided by a limited battery. Therefore, energy efficiency turns into one of the biggest concerns in the design of electronic portable devices [5]. Multimedia processing takes the lion's share of the overall processes in electronic portable devices. Applying imprecise computing methods in such applications bring advantages, including decreasing the hardware complexity, reducing the power dissipation as well as enhancing the performance [6,7]. Digital signal processors (DSPs) offer brilliant computing platforms for multimedia processing due to their superior performance, high levels of integration and low-power consumption [8]. As a matter of fact, arithmetic circuits are the major blocks of DSP and multiplier is one of the foremost, frequently used and critical arithmetic blocks. Therefore, enhancing the performance and energy-efficiency of multiplier block has a significant impact on the performance of the electronic portable devices. Multiplication is composed of three steps: in the first step, the partial products are generated from "multiplicand" and "multiplier. In the second step, the partial products are reduced to only two operands in a carry-free structure. Finally, in the third step, a fast addition is conducted to yield the final result. Among these steps, the second one utilizes the most chip area, consumes a large amount of power and contributes to the maximum propagation delay compared to the rest of the blocks [9]. The partial product reduction techniques such as Wallace and Dadda suffer from VLSI irregularity due to using only full and half adders [2]. Compressors can be utilized instead of full adders in order to enhance the circuit regularity and reducing the latency as well as the power consumption of the partial product reduction stage. 4:2 compressor structures are preferred to other compressor degrees, due to lower complexity as well as premier regularization [10]. Therefore, designing an efficient 4:2 compressor has attracted much more attention from researchers. This led to several contributions in the literature, considering the critical path, area and power consumption reduction of this vital arithmetic block. These contributions, comprise the design of 4:2 compressor both in precise and imprecise structures

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in a variety of technologies [9–16]. In this paper, we also introduce a novel circuit for imprecise 4:2 compressor design. Similar to [16], for the realization of the proposed imprecise 4:2 compressor, two well-known devises in the nano era are considered. FinFET as the prevailing technology of today's industry with significant features such as smaller drain induced barrier lowering (DIBL), smaller subthreshold swing, and higher I_{on}/I_{off} [17,18], and Quantum-dot Cellular Automata (QCA) as an emerging technology with promising features like ultra-high density, very low power consumption, and significant switching speed for future VLSI industry [19,20]. The underlying idea behind all realization is the adoption of more simplified logic expression considering the VLSI features of the aforesaid technologies. The proposed design results in a significant saving in terms of area occupation, power dissipation as well as propagation delay in both targeted technology.

The rest of this paper is organized as follows. In Section 2, a review of the related works is conducted. In Section 3, a logical description of the proposed imprecise 4:2 compressor is presented based on the majority gate. The VLSI realization of the proposed 4:2 compressor is also detailed for both FinFET and QCA technologies. In Section 4, the performance of the proposed 4:2 compressor is evaluated against the related state-of-the-art. For this purpose, for each technology, its specific performance criteria are considered. In addition, as in the design of imprecise structures, the compromises between the output error and other performance criteria are considered. As a case study, the application of image processing based on the multipliers with imprecise compressors is considered. Finally, Section 5 concludes the paper.

2. State-of-the-art

Regardless of whether the designs are special to precise or imprecise 4:2 compressors, a wide range of silicon FET (MOSFET or FinFET) based compressors based on two important logic blocks; AND/OR gate and Exclusive OR/NOR gate have been realized in the literature. The former suffers from high circuit complexity and the latter suffer from high power consumption due to high switching activity. The presented structures in [9–11] are the examples of precise 4:2 compressors based on XOR and AND/OR logical gates. The imprecise 4:2 compressors in [14] are originated from the modification of the truth table of precise 4:2 compressor considering the weight of the output nodes. The aforesaid designs have significantly improved the performance metrics such as transistor counts, power consumption, and the propagation delay compared with the precise 4:2 compressors. In [15] the authors presented 4:2 compressors with the ability to switch between exact and inexact modes. The structure of these compressors includes an imprecise compressor as well as a redundant block. In the inexact mode, the redundant part is gated via the transistors which are connected to the power supply. In the exact mode, co-operation of the imprecise compressor and redundant part is led to yield the precise values of the 4:2 compressor at the outputs of the circuit. The three-state buffer gates in the outputs of the circuit, as well as some transistors, are utilized in order to isolate the exact and inexact operation modes. In contrast to mentioned imprecise 4:2 compressors, the authors in [16] for the first time contributed based on the *Majority* gate to achieve a more efficient design. The following equations describe the proposed imprecise 4:2 compressor in [16].

$$\begin{aligned} C_{out} &= X_3 \\ Carry &= X_4 \\ Sum &= Maj\left(X_1, X_2, \overline{Maj}(X_3, X_4, C_{in})\right) \end{aligned} \tag{1}$$

Using such logic in Nano-scale silicon FET structures, like FinFET, brings more energy efficiency and reliability to arithmetic circuits compare to the XOR-based approaches [22]. Moreover, the implementation of 4:2 compressors in the majority (or minority) based emerging technologies using abovementioned AND-OR and XOR logic gates leads to dramatic performance degradation. To show the importance of this issue, the author in [16] considered QCA as one of the promising majority based emerging technologies for designing the imprecise majority based 4:2 compressor. Majority gate as the basic building block in the QCA technology has an effective implementation. Consequently, as expected, the realization of the imprecise 4:2 compressor in [16], based on the QCA technology, has an acceptable simplicity and high degree of performance from the perspective of a wide range of standard performance evaluation metrics in the aforementioned technology.

3. Proposed imprecise 4:2 compressor

In this paper similar to [16], in order to cope with the problems that arise from the realization of the imprecise 4:2 compressor based on XOR and AND-OR gates, the majority-based approach also is considered. Thus, the architecture of proposed imprecise 4:2 compressor will be appropriate for both FinFET-based structures as the current technology in the industry and QCA technology as the emerging majority gate based structure for the future of the semiconductor industry. We would like to stress that in the silicon FET based structure, the design procedure should be based on reducing the number of transistors in the critical path and the capacitors of the intermediate nodes, which will consequently decrease the switching capacitance as well as the charge and the discharge paths of the output nodes [21]. Meanwhile, in the design of QCA-based structures, an approach of reducing the complexity of the circuit, in terms of area, number of cells, number of layers, as well as the number of clock cycles, brings more efficiency in the performance metrics such as power dissipation and latency [20]. The main idea behind the proposed approach for the above-mentioned technologies is to reduce the hardware complexity as well as the circuit latency at the expense of imposing more negligible error compared to [16]. Similar to the presented imprecise 4:2 in [16], the proposed design also employed 3-input majority gate. The following equation explains the logic of the proposed imprecise 4:2 compressor.

$$\begin{aligned} C_{out} &= Maj(X_1, X_2, X_3) \\ Carry &= X_4 \\ Sum &= C_{in} \end{aligned} \tag{2}$$

According to (1) and (2), the difference between the proposed design and the design of Moaiyeri et al. [16] is in generating the C_{out} and *Sum* output signals, whereas the *Carry* output is similar in both designs. The performance of the presented imprecise compressor is affiliated to the performance of C_{out} signal generator block, while in the design of Moaiyeri et al. [16] the performance is interdependent to the performance of *Sum* signal generator block. The other 4:2 compressors outputs (*Carry* and *Sum* outputs in the proposed design and *Carry* and C_{out} outputs in the design of Moaiyeri et al. [16]) are directly generated by input signals without any hardware components employment. As a result, considering the fact that the C_{out} signal generator of the proposed circuit (C_{out}) imposes fewer hardware costs to the imprecise 4:2 compressor structure in comparison with the *Sum* generator of the design of Moaiyeri et al. [16], the proposed circuits brings less complexity to a given imprecise multiplier. On one hand, the proposed design has fewer counts of majority gates (one majority gate in comparison to two majority gates of design [16]) and on the other hand, the fewer logical stages are expected to generate the output (one majority gate stage in comparison with two stages of majority gate). Fig. 1 illustrates the schematic of the proposed imprecise 4:2 compressor.

The truth table of the proposed imprecise 4:2 compressor, as well as the precise 4-2 compressor, is illustrated in Table 1. ED (error distance) is explained as the arithmetic distance between