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# A highly stable reliable SRAM cell design for low power applications

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ABSTRACT

The growth in demand for power-efficient neural network accelerators has generated an intense demand for low power static random access memory (SRAM). In this context, a power-efficient transmission gate based 9-Transistor (TG9T) SRAM bitcell has been proposed in this work. In order to assess the relative performance of the proposed design in terms of major design metrics, it has been juxtaposed with contemporaneous designs such as the feedback-cutting 7T, fully differential 8T (FD8T) and single-ended disturb free 9T (SEDF9T) bitcells, while the reliability of such SRAM designs when subjected to process variations has also been analyzed. In terms of read stability (RSNM), the TG9T shows 2.87×/3.36× higher RSNM and 2.90×/2.67× narrower spread in RSNM, respectively, as compared to 7T/FD8T. In addition, it also exhibits 1.4×/6.55× higher write ability (WSNM) and 1.01×/5.05×/1.06× narrower spread in WSNM when compared with FD8T/SEDF9T and FD8T/SEDF9T/7T respectively. Moreover, a 1.15×/1.06× narrower spread in read delay ($T_{RA}$) and 1.54×/1.38× narrower spread in read current ($I_{READ}$) are also exhibited by the proposed design in comparison with 7T/FD8T. The reliable nature of TG9T is indicated by the narrower spread in read stability, write ability, read delay and read current. Furthermore, in comparison with 7T/FD8T, TG9T consumes 2.92×/1.04× lower hold power. Additionally, the proposed cell shows 10.80×/17.81× lower write power consumption and 1.43×/18.37× lower read power consumption when compared to that of SEDF9T/FD8T and 7T/FD8T respectively. Amongst all SRAM bitcells used for comparison, the proposed bitcell yields the lowest $V_{DD,min}$. The TG9T cell achieves all the aforementioned improvements at the cost of 1.22×/1.34× longer $T_{WA}$ and 1.93×/1.93× longer $T_{RA}$ when compared with 7T/SEDF9T and 7T/FD8T, respectively, at a supply voltage of 0.7 V.

## 1. Introduction

The recent advances in the fields of machine learning algorithms and artificial intelligence have led to development of newer and smarter devices, which not only reduce the burden of human involvement but also bring with themselves an amount of intelligence, which was hitherto unseen. Their applications include facial recognition [1], speech recognition [2], and video surveillance amongst many others.

Such progress has been made possible by the vast amount of data available today which are used by underlying neural networks to train themselves as well as their high-performance processors (called accelerators). Conventionally, a neural network accelerator is composed of a processing element and an on-chip buffer on a dedicated application-specific integrated circuit (ASIC) to ensure that it is capable of supporting multiple workloads and is energy-efficient [3]. In addition, the accelerator also employs an off-chip memory for storage of large amount of data, usually in the form of dynamic random access memory (DRAM) [4]. However, the DRAM is relatively slow and to bridge the gap, a static random access memory (SRAM) based global buffer is used as an on-chip memory. Since SRAMs are relatively fast, data is first transferred onto the on-chip memory from the off-chip memory, which is followed by its retrieval to the processing element [4]. Moreover, extended applications of machine learning algorithms like “edge computing” require devices with extended battery lives as they are “always-on” [5]. Therefore, the design of SRAM cells with low dynamic power consumption is required for neural network accelerator implementations.

Since, dynamic or active power reduces quadratically with decrease in supply voltage ($V_{DD}$) [6], downscaling of $V_{DD}$ is a popular way to achieve power-efficiency in SRAM design. Moreover, static power, which makes up a significant share of aggregate power dissipation, reduces linearly with decrease in $V_{DD}$ [7]. Therefore, supply voltage scaling results in reduction of cumulative power dissipation of SRAM cells.

On the other hand, operational delay increases with downscaling of $V_{DD}$, which leads to a considerable amount of increase in total energy

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per read/write cycle [8]. In addition, noise margin is significantly deteriorated since the difference between $V_{DD}$ and threshold voltage ($V_t$) decreases, rendering the circuit vulnerable to operational failure [9]. Additionally, the stability of the design is severely degraded owing to the prevalence of random dopant fluctuations (RDF) as well as random process, voltage and temperature (PVT) variations in the sub-micrometer domain [10].

Consequently, designing an SRAM cell which is capable of overcoming the aforementioned challenges as well as performing reliably is imperative for the realization of power-efficient accelerator memory.

The conventional 6T SRAM cell, while operating at low $V_{DD}$, is vulnerable to frequent read upsets owing to its degraded read static noise margin (RSNM) [11]. Similarly, the inability of the 6T bitcell to consistently preserve the device strength ratio at reduced supply voltages, may render it incapable of reversing the stored data and lead to frequent write failures.

In order to overcome the limitations faced by the conventional design as well as to obtain improved results, several designs have been proposed in the past couple of decades. Considerable improvements in read stability is exhibited by bitcells proposed in [12,13] due to the use of separate discharging path during read operation, which isolates the cross-coupled inverters from bitlines. Moreover, low leakage power dissipation is shown by the LP8T [11], LP10T [12] and LP9T [13] cells owing to the presence of an additional tail-transistor in their core cell.

However, for all their improvements, they exhibit very high dynamic power consumption. Since, in single-ended bitcells, the activity factor of bitline switching is reduced below 0.5 [14], the use of single-ended structure may appear to be the most efficient way of reducing dynamic power consumption. However, such a single-ended SRAM bitcell is incapable of performing the '1' writing operation in absence of any technique which enhances the writing mechanism [15].

Thus, to ensure a successful '1' writing operation, several write-assist techniques have been adopted by different single-ended bitcells in [14–20]. Considerable improvements in write ability, which is estimated in terms of write static noise margin (WSNM), is obtained by the 7T [14] and 9T [16, 17] cells by employing a feedback cutting transistor inside their core bitcells. However, bitcells in [14,16] are highly susceptible to read upsets in absence of any decoupling mechanism. Moreover, while the 9T bitcell in [17] shows enhancement in RSNM due to the application of read-decoupling mechanism in addition to a strengthened write ability, the half-selected bitcells are susceptible to PVT variations. By using asymmetrical inverter sizing in the core bitcell, bitcells in [15,18] exhibit enhancement in WSNM. However, these bitcells are highly prone to failure when subjected to PVT variations. Although, the single-ended disturb-free 9T (SEDF9T) [19] cell exhibits improvement in write ability due to the use of negative bitline scheme, it is incapable of achieving a low $V_{DD,min}$ upon being subjected to process variations. The single-ended 7T bitcell in [20] is read-disturb free and employs an additional series-stacked transistor in one of its inverters to enhance the write ability. However, it exhibits a substantially degraded hold stability (HSNM) [21]. Although, asymmetrical inverters are used in the core bitcell of a dual $V_t$ SRAM bitcell in [22], the complexity of fabrication is significantly increased. Improvements in both RSNM and WSNM are exhibited by a Schmitt trigger based SRAM bitcell in [23], a data aware power cutoff (DAPC) SRAM bitcell in [24], a write assist low power 11T (WALP11T) SRAM bitcell in [25] and a dynamic loop-cutting write assist 12T (DWA12T) in [26], which also show robustness upon being subjected to harsh process variations. However, their dynamic power consumption is significantly high and their fabrication leads to a significant area overhead [21].

In order to overcome the aforementioned limitations, we propose a transmission gate based 9-Transistor (TG9T) SRAM bitcell (see Fig. 1) in this work. The proposed bitcell improves read stability and enhances the write ability simultaneously. In addition, it also reduces consumption of dynamic/active power and static power. The contributions of this work are as follows:

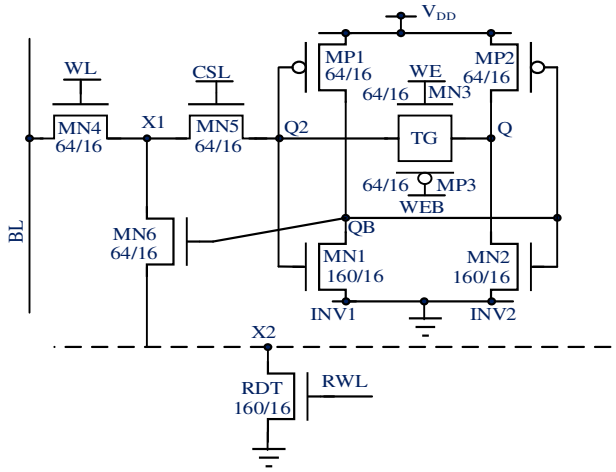


**Fig. 1.** Schematic of proposed TG9T SRAM cell.

1) A significantly enhanced write ability (WSNM) is obtained by the proposed bitcell owing to the use of feedback cutting mechanism in the cross-coupled inverters during write operation.
2) An optimum read stability (RSNM) is exhibited by the proposed bitcell due to the use of a single-ended decoupled-read technique.
3) A considerable reduction in consumption of dynamic power is achieved owing to the presence of a single bitline.
4) Consumption of leakage power is also minimized due to transistor stacking in discharge path of the proposed bitcell while operating in standby mode.
5) The reliable nature of the proposed bitcell is reflected by exhibiting a narrower spread in RSNM, WSNM, $T_{RA}$ and $I_{READ}$.
6) Amongst all comparison bitcells, TG9T exhibits the lowest $V_{DD,min}$.

The various sections, into which this paper is divided, are as follows. The proposed cell is described and its operations are discussed in Section 2 while Section 3 gives the comparative study of TG9T in terms of various design metrics under harsh PVT variations, with several state-of-the-art comparison bitcells. A comprehensive summary of the different comparisons performed in this work are provided by Section 4 and the $V_{DD,min}$ analysis is given by Section 5. Section 6 serves as the conclusion to this work.

## 2. The proposed TG9T bitcell and its operation

The schematic diagram of the proposed bitcell is shown in Fig. 1. It can be seen that the inverter INV1/INV2, inside the core bitcell of TG9T, is formed by the pull-up transistor MP1/MP2 and pull-down transistor MN1/MN2. MN3 and MP3 constitute the feedback cutting transmission gate (TG), which is placed between INV1 and INV2 to disconnect the cross-coupled feedback path. The wordline (WL), which is row-based in nature, turns ON the access transistor, MN4, while the column-select-line (CSL) turns the write access transistor, MN5, ON. A single columnar bitline (BL) is connected to MN4. The read decoupling transistor, MN6, which is gated by storage node 'QB', is placed between the X1 node and the X2 node. The simplified memory architecture of the proposed bitcell is shown in Fig. 2. A row-based read discharging transistor, RDT, which is shared by each bitcell in a row, connects MN6 to GND. A row-based control signal, RWL, is used to activate the RDT during read operation. The different signals applied during distinct operations of the proposed bitcell are reported in Table I.

### 2.1. Write operation with feedback-cutting mechanism

During the write operation, MN4 and MN5 are turned ON by activating row-based WL and columnar CSL, respectively. RDT is