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A 7b 400 MS/s pipelined SAR ADC in 65 nm CMOS

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ABSTRACT

This paper presents a 7-bit 400-MS/s pipelined successive approximation register (SAR) analog-to-digital converter (ADC) with high reliability. To meet the high demand for medium resolution and high sampling speed, a modified switching scheme is adopted to resolve charge leakage problem and to improve the reliability of SAR ADC. Compared to the conventional architecture, the modified bootstrapped switch which uses two sampling MOSFETs is employed to increase the uniformity of sampling voltage and save the chip area. In addition, three parallel comparators are controlled by a novel asynchronous clock generator to minimize the latching error. The measurement result shows that the ADC, implemented in the 65-nm CMOS process, achieves the 40.83 dB signal-to-noise and distortion ratio (SNDR) and 64.75 dB spurious-free dynamic ranges (SFDR) at 400-MHz sampling frequency without additional digital calibration.

1. Introduction

With the development of mobile communication toward 5th generation wireless systems, communication systems put forward higher demand for ADCs with ultra-high speed, medium resolution and low power consumption. Considering the following type of ADCs: flash ADC is the fastest but sacrifices a lot of power and area; pipelined ADC can achieve high speed and precision, but it still has high power consumption due to the existence of inter-stage operational amplifier; the SAR ADC has the advantages of low power consumption and high accuracy, but its quantization speed is slow. Based on these structures to realize an ADC with high performance and low power consumption has become a key challenge. Although time interleaving technique has been adopted in many papers [1,2] to greatly improve quantization speed, the increasing number of channels makes the impact of inter-channel mismatch on quantization accuracy more serious. So, a single-channel ADC with high quantization speed is also required in time interleaved ADC. Many mixed structures are proposed by combining the advantages of various structures and suppressing the shortcomings as much as possible, which meet the application requirement. Multi-bit per cycle conversion is the advantage of flash ADC, and pipeline SAR ADC [3] also achieves a high performance. Therefore, an ADC combined the two structure above can greatly improve the overall performance of the converter.

In the published papers [7–10], multi-bit per cycle technique has demonstrated its advantages of speed. The 2b per cycle means that the ADC converter can produce two comparison results in a comparison cycle. A 2.4 GS/s SAR ADC in Ref. [8] with 1-then-2b/cycle conversion scheme is proposed to realize 7 bits resolution. A 2b/cycle SAR ADC in Ref. [9] achieves 6-bit and 1.35 GS/s quantization speed. In Ref. [10], an SAR ADC with 2b/cycle in 65 nm CMOS resolves 8 bits at 400-MHz sampling frequency.

However, due to many non-ideal factors not taken into account, there are also many reliability problems in the relevant papers. In Ref. [8], the 1-then-2b/cycle conversion scheme is suitable for the background offset calibration, but the residual voltage drops to a voltage lower than GND, leading to the charge leakage. Many comparators are employed in Ref. [9] to resolve 2-bit in one comparison, causing larger power consumption and mismatch problems. Using independent bootstrapped switches to sample the same signal in Ref. [10], there will be some discrepancies between the sampled voltages on different capacitor arrays. Consequently, all the non-ideal factors reduce performance advantages of the new structure.

In order to address the above issues, this paper analyzes the conventional circuit and switching scheme in detail, and some solutions are given out in the proposed pipelined SAR ADC. The paper is organized as follows. Section 2 briefly illustrates the architecture of the proposed pipelined SAR ADC. Section 3 analyses the inaccuracy factor and put forward relevant solutions. The chip microphotography and measurement results of the ADC are described in Section 4. Section 5 concludes this paper.

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2. Architecture of the proposed pipelined SAR ADC

Fig. 1 shows the conceptual block diagram of the pipelined SAR ADC in this paper. In order to restrain the unreliability and improve the speed of SAR ADC in traditional architecture, the 1-then-2b/cycle technique proposed in Ref. [8] is adopted. Fig. 2 demonstrates the operation timing of the proposed Pipelined SAR ADC. Following by the second comparison, the sampled differential signal can realize 3-bit rough quantization in two comparison cycles. Then a multiplying digital-to-analog converter (MDAC) circuit with a high-performance operational amplifier, sharing the partial capacitor arrays with the first-stage SAR ADC, is applied to realize the double amplification of residual signals. After that, the second-stage SAR ADC will finely quantify the amplified residual signals to resolve 5-bit quantization code. Finally, a 7-bit resolution can be obtained through the digital output of two-stage ADC being encoded by the digital error correction circuit.

As the key function module of pipelined ADC, the gain and load of MDAC are higher than the traditional pipeline ADC, which requires higher gain and bandwidth operational amplifiers to ensure accuracy and conversion speed. In a word, the design of MDAC circuit is very important. In order to improve the quantization accuracy and reduce power consumption, the redundant bit correction technique [4] and gain halving technique are applied in this design, reducing the inter-stage gain from 2^3 to 2. These techniques reduce the output amplitude and open-loop gain of the operational amplifier, thereby making the circuit easier to be designed. Because of the negative feedback structure, the open-loop gain needed must be greater than 41 dB. In addition, in order to achieve signal amplification in 700 ps, the GBW of the operational amplifier is required to be greater than 1.8 GHz. To meet the requirements of gain and signal swing, the two-stage operational amplifier achieves 2.1 GHz GBW and a gain of 45 dB.

3. Analysis and solution of inaccuracies

In order to resolve the inaccuracies of the SAR ADC in this paper, the effects of non-ideal factors on ADC performance are analyzed in detail from the aspects of switching scheme, control of the comparator and sampling circuit, and corresponding solutions are proposed respectively.

3.1. Charge leakage

In the traditional 2b/cycle structure, the switching scheme is critical to the overall quantization process. The various switching schemes result in different degree of charge leakage. The probabilistic charge leakage problem is that the voltage on the top plate of capacitor changes imperfectly due to the pre-charge operation, and this voltage can be expressed as :

$$V_{top} = V_{sampled} - \frac{D_1}{2}V_{cm} - \frac{D_2}{4}V_{cm} - \frac{D_3}{8}V_{cm} \quad (1)$$

where D_1, D_2 and D_3 may be "0" or "1" respectively. When the sampled signal $V_{sampled}$ is relatively small (especially close to GND), the negative voltage V_{top} will drive the sampling MOS transistor to enter the subthreshold region in the holding phase, thereby leading to the charge leakage. The charge leakage affects the accuracy of quantization results, even leading to error codes directly.

The cause of charge leakage has been introduced above, so the switching scheme should be used carefully for different quantization circuits. Three conventional switching schemes suitable for the 2-bit/cycle SAR architecture are as follow: a) monotonic switching scheme [5] with addition pre-charge operation; b) monotonic switching scheme with subtraction pre-charge operation; c) Vcm-based [6] multi-bit switching scheme.

When these switching schemes are applied in 2b/cycle conversion scheme, the residual signal generated in the normal quantization process is illustrated in Fig. 3. As can be seen from the figure, the pre-charge operation before every comparison is needed. When the full swing input signal is taken into account, the residual signals shown in Fig. 3(a) are always higher than GND. So, there is no charge leakage. However, the figure also demonstrates that the change of the residual signals results in the unstable common-mode voltage, which increases the mismatch between the parallel comparators and limits the application of this switching scheme in the multi-bit per conversion architecture of two-stage SAR ADC.

The residual signal depicted in Fig. 3(b) demonstrates that some of them become lower than the input signal after the initial pre-charge operation. If the input signal is close to GND, the minimum residual signal will be a negative voltage, leading to a charge leakage. Besides, the common-mode voltages of the residual signal also change all the time and are getting lower than Vcm. Similarly, the residual signal in Fig. 3(c)

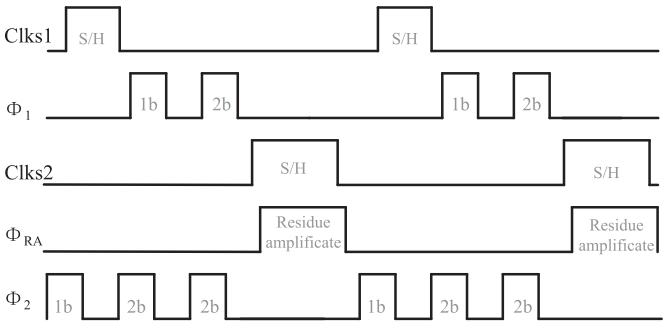

Fig. 2. Operation timing of the proposed Pipelined SAR ADC.

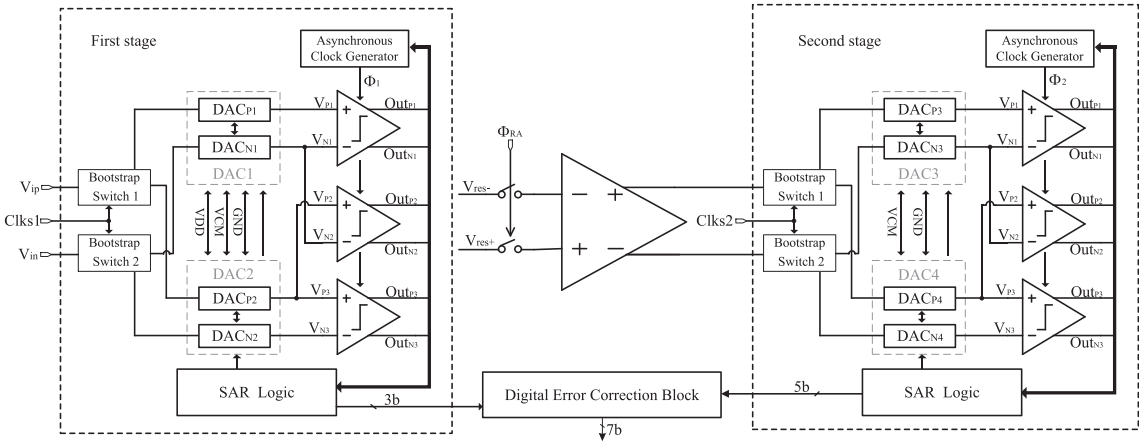

Fig. 1. Proposed Pipelined SAR ADC architecture.