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Two-step synthesis of few layer graphene using plasma etching and atmospheric pressure rapid thermal annealing

A.R. Graves, S. Chaudhari, C.D. Stinespring*

Department of Chemical Engineering, West Virginia University, Morgantown, WV 26506-6102, United States of America

A B S T R A C T

A two-step process using halogen based plasma etching combined with atmospheric pressure rapid thermal annealing has been used to synthesize few layer graphene films on 6H-SiC (0001) surfaces. In this process, the 6H-SiC substrates were etched under different plasma conditions to produce a carbon rich surface layer. This was followed by rapid thermal annealing in a flow of atmospheric pressure Ar to produce the graphene films. The effects of different etching conditions, heating rates, and average and maximum annealing temperatures were investigated. Changes in surface and near-surface composition after each step were characterized by x-ray photoelectron spectroscopy and overall film quality was assessed using Raman spectroscopy. Film defects associated with this synthesis method included a buffer layer between the SiC substrate and graphene as well as oxygen-based defects on the graphene surface. Electrical characterization of these films was performed using both two and four point methods. In the two point measurements, these films exhibited back-to-back Schottky behavior from which the Schottky barrier height, carrier density and mobility were determined. The four point measurements were used to determine the contact and film resistivity as well as the transfer length.

1. Introduction

A variety of graphene synthesis methods have been investigated and reported extensively in the literature. These include mechanical [1] and chemical [2] exfoliation as well as chemical vapor deposition [3,4]. In addition, thermal sublimation of Si from SiC by ultrahigh vacuum (UHV) [5] and atmospheric or near atmospheric pressure annealing [6,7] have also been used to synthesize graphene. Of these methods thermal sublimation is of interest because of the potential for wafer scale fabrication on an electrically insulating wide bandgap substrate such as SiC [8–10]. Because of the importance of the scalability issue and the utility of SiC as a substrate, we have previously investigated alternatives to the sublimation process. Specifically, this work focused on the synthesis of graphene on SiC using halogen based plasma etching followed by ultrahigh vacuum annealing (UHVA) to form graphene [11].

In our previous work, Raghavan et al. [11] showed that both Cl_2- and CF_4-based inductively coupled plasma-reactive ion etching (ICP-RIE) of 6H-SiC (0001) surfaces could be used to selectively etch Si from the 6H-SiC (0001) surface and near surface layers. This produced a C-rich layer that could then be annealed under UHV conditions to form few layer epitaxial graphene films. The number of graphene layers was shown to be directly proportional to the RIE power. These films reproducibly had an average thickness of one to four layers depending on the plasma etching conditions. While this process works quite well, it requires use of UHV conditions which may increase processing costs and complexity.

This paper reports an investigation on the effects of replacing the UHVA process with an atmospheric pressure rapid thermal anneal (RTA) in a flow of Ar gas. Specifically, the effects of the heating rate, the average annealing temperature, and the maximum annealing temperature are considered in detail. As in prior studies, it is shown that the plasma etching condition may be used to reproducibly control the film thickness. The major film defects, their implications for the growth process, and their effects on the electrical properties of the films are described as well.

2. Experimental

The 6H-SiC used in this study was purchased as 2 in. wafers from University Wafer, Inc. Prior to graphene synthesis, the wafers were cut into 1 cm × 1 cm substrates using a Discotech Model DAD3240 wafer dicer. These were degreased for 5 min using acetone and methanol. This was followed by blow drying in ultrahigh purity N_2. These substrates were plasma etched using a Trion Technologies Minilock-Phantom III ICP-RIE system using a CF_4 based plasma. The ICP power was maintained at 600 W, while the RIE power was varied over the range of 100 W to 500 W in parametric studies of the etch process. As discussed later, the RIE power was used to control the number of graphene layers produced. Typical process conditions were 20 sccm CF_4 flow and 25 mTorr pressure. At 600 W ICP and 400 W RIE power, a nominal etch rate of 200 nm/min was observed. The substrates were typically etched

* Corresponding author.
E-mail address: cstinesp@wvu.edu (C.D. Stinespring).

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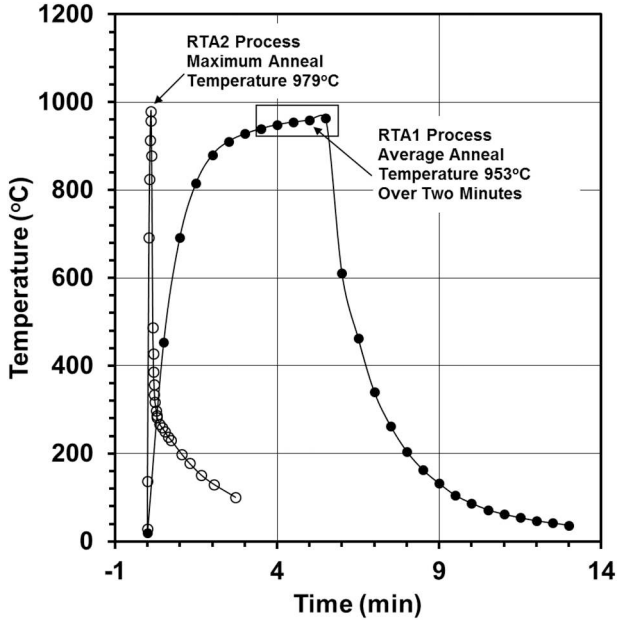

Fig. 1. Typical temperature vs time profiles for RTA1 and RTA2 annealing processes. This illustrates the marked difference in heating rates. For the RTA1 process, the rectangular insert corresponds to the portion of the profile associated with the anneal.

for 12 min which corresponds to a depth of 2.4 μm under these conditions. This resulted in a planarized surface well below the depth of any expected polishing damage [12].

Following ICP-RIE, one or more of the etched substrates (typically less than three) were placed in the RTA setup. This consisted of a 0.5 in. OD quartz flow tube with Ultra-Torr (Swagelok) fittings. The tube was continuously purged with Ar (Airgas Research Plus) for which the total impurities did not exceed 3 ppm (N_2 ~2 ppm, total hydrocarbons ~0.1 ppm, and O_2, H_2O, CO, and CO_2 totaling ~0.5 ppm). Typical Ar flow rates were on the order of 100 sccm. A type K thermocouple housed in a quartz thermocouple shield located adjacent to the substrate position was used to monitor the temperature of the substrates.

Using this setup two different RTA processes were studied. In the first, referred to as RTA1, the tube furnace was brought to a steady temperature (e.g. 1000 °C) slightly above the desired annealing temperature (e.g., 950 °C). The quartz tube was then inserted into the furnace, and the rapid temperature increase of the samples was measured using the thermocouple. A typical temperature versus time profile for the RTA1 process is shown in Fig. 1. Once the temperature reached 99% of the target anneal temperature (e.g., 940 °C in this case), the "anneal clock" was started and continued for the desired anneal time. In the case of a two minute anneal time shown here, the maximum recorded temperature was 960 °C and the average temperature was 953 °C. This is within the nominal limits of accuracy for the thermocouple (± 0.4%) [13]. After the desired annealing time, the tube was withdrawn to allow rapid cooling of the substrates, and upon reaching room temperature, the annealed substrates were removed for characterization.

For the RTA1 process, heating rates were limited due the need to have the heater temperature only slightly higher than the nominal anneal temperature. For the case shown in Fig. 1, the initial heating rate was on the order of 4.5 °C/s which was typical of all the RTA1 data discussed here. Moreover, increasing the anneal time for a given heater temperature always lead to higher average and maximum anneal temperatures. To gain insight into the effects of heating rate and maximum anneal temperature, a second RTA process referred to as RTA2 was devised.

For the RTA2 process, the heater was brought to a steady temperature of 1400 °C. The quartz tube with samples was then rapidly inserted into the furnace, and the temperature was allowed to increase to a desired maximum temperature. The tube was then quickly withdrawn, and the samples were allowed to cool. A typical temperature versus time profile for the RTA2 process is shown in Fig. 1. Here the heating rate is on the order of 140 °C/s.

Although both annealing approaches are easily reproducible, it is difficult to independently vary the heating rate, anneal time, and anneal temperature. From the temperature versus time profiles shown in Fig. 1, however, it is clear that the two methods differ considerably in heating rate, and a direct comparison of samples heated to the same average temperature (RTA1) and maximum temperature (RTA2) provides at least a qualitative assessment of overall differences due to heating rate.

Following each process step, x-ray photoelectron spectroscopy (XPS) and Raman spectroscopy were used to analyze the substrate and/or thin film. The XPS measurements were obtained using monochromated Al-K_α x-rays ($h\nu = 1483.6$ eV) using a PHI 5700 system with an Omni Focus V lens. In most cases, the XPS spectra were acquired in the "bulk analysis mode" in which electrons ejected at 45° relative to the surface normal were analyzed. In some cases, however, greater surface sensitivity was achieved using the "surface analysis mode" in which electrons ejected at 95° relative to the surface normal were analyzed. For this instrument, the analysis spot size could be varied, but for the results reported here a spot size of 100 μm was used. Typical power levels were ~25 W. Raman spectra were acquired using a Renishaw micro-Raman system with a 532 nm laser having a power level was 100 mW and spot size of 25 μm. This resulted in a nominal power density of 0.2 mW/μm^2. For both XPS and Raman, multiple spots were analyzed on each sample to assure consistency.

Attenuation of the substrate (SiC) C1s photoelectron peak by the graphene overlayer was used to determination the thickness of the graphene. This was accomplished using a simple layer model described previously by Yates and coworkers [14] and used in our previous studies of UHV annealing of graphene on SiC [11]. A similar approach has been used by others to characterize the thickness of graphene films formed on SiC [15–17]. The details of this model are given in the supplemental material.

The electrical properties of the graphene films were characterized using both two and four point measurements. For these measurements, the 1 × 1 cm graphene on SiC films were diced into 2.33 mm wide strips. For each strip, 30 nm/100 nm thick Ti/Au contacts 2.33 mm wide × 0.71 mm long were deposited with different lateral separations. These included two terminal contacts (i.e., a contact at both ends of the strip) and four additional contacts at intermediate distances. This was accomplished using a K.J. Lesker custom built LAB 18 e-beam evaporator and homemade shadow masks. To improve the durability of the test samples and improve reliability and reproducibility of the electrical measurements, the Ti/Au contacts were mounted on model HDR00823 transistor outline headers provided by Spectrum Semiconductor Materials, Inc. and wire bonded to the header pins using a West Bond 74776E wire bonder. Electrical measurements were made with a Keithley 4200 Semiconductor Characterization System.

3. Results and discussion

Fig. 2 shows survey spectra for as received, ICP-RIE etched, and etched and annealed 6H-SiC (0001) surface. The etching was done under the standard conditions described above with ICP power at 600 W and RIE power at 300 W. The sample was annealed for 2 min at 970 °C with an RTA1 profile similar to that shown in Fig. 1. For the as received sample the relative intensities of the Si2s and C1s peaks are representative of the near stoichiometry of the SiC surface.

After ICP-RIE etching, there is a slight increase in intensity of the C1s relative to the Si2s peak as well as a broadening of the C1s peak. In addition, O1s, F1s and a very low level N1s peak can be observed. The