

Bias stress effect on high mobility-hysteresis free pentacene-based organic thin film transistors

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ABSTRACT

Fabrication and characterisation of pentacene-based top contact organic thin film transistors (OTFTs) with poly(methyl methacrylate) (PMMA) as the dielectric layer have been investigated. Stability of OTFTs was also investigated as devices were retested after 12 months of fabrication. The effects of bias stress on the OTFTs are studied and modelled for different stress conditions (different gate and drain bias stress measurements and stress times). The effects of bias stress have been expressed in terms of the shift in threshold voltage ΔV_T for a given stress condition. The shifts in threshold voltage has been analysed for different gate–source and drain–source voltages. The devices have demonstrated a negligible hysteresis in both the transfer and output characteristics of the OTFTs due to application of stress voltage, indicating traps-free interface between the pentacene and PMMA.

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1. Introduction

Organic materials have attracted special attention in the last decade due to their remarkable characteristics and potential applications in flexible electronics. Most of these organic materials have an inherent flexibility, which make them viable for use on flexible substrates without developing stress fractures or losing their electronic characteristics. This has allowed for the development of new generation of electronic devices based on polymers or small molecular materials. Such devices have attracted interest from both academic and industrial researchers due to their low cost, low temperature processing and mechanical flexibility. Applications such as organic solar cells [1], light emitting displays [2], organic field-effect transistor [3] and sensors [4] are all rather in advance stages of research.

Pentacene-based thin film transistors (TFTs) have attracted much interest for large area electronics applications; this is due to its high performance which is comparable or even better than amorphous silicon (a-Si:H) [5,6]. Such electrical performance is sufficient for many applications such as backplanes of organic light-emitting diode displays [7], imagers [8], and conformal large-area arrays of pressure and temperature sensors [9]. Although sufficient mobility has been achieved with organic transistors for various

applications, it has been reported that the current–voltage (I – V) characteristics change with the application of prolonged voltages [10–12]. Such change is termed the “bias-stress effect”. Understanding the bias stress effect is important for practical circuit applications. The bias stress effect is attributed to the trapping of channel carriers in electronic (positive) charges; these trap states located in the gate dielectric, or at the semiconductor/dielectric interface [6,13].

Here, we report the optimum fabrication of, high field-effect mobility, pentacene-based OTFTs. In order to measure the endurance properties of these OTFTs, the effect of bias stress for different stress conditions is investigated in this study. We applied bias stress on the devices after more than one year of fabrication. This was carried out by first applying a constant gate bias at different stress times. In the second test different gate bias stress values were applied at a constant stress time and finally we applied a constant gate bias at constant stress time with different drain bias stresses.

2. Experimental details

The following materials were purchased from Sigma–Aldrich: PMMA (molecular weight 93,000), anisole and pentacene. All device fabrications were carried out in a class 1000 clean room. The fabrication of OTFT devices with the structure of Al/PMMA/pentacene/Au (as shown in Fig. 1) was achieved by thermal evaporation of 50 nm layer of Al through a shadow mask on

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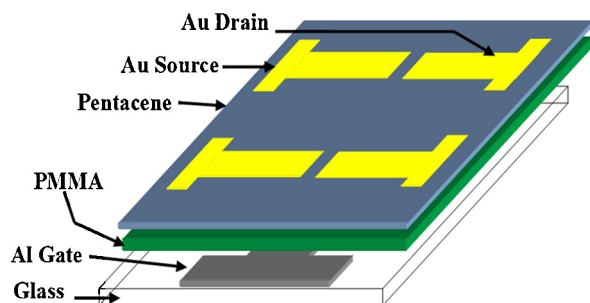


Fig. 1. Schematic diagrams of the pentacene-based OTFTs.

glass substrate as the gate electrode. A 300 nm thick insulating layer was deposited by spin coating of 10% (wt) anisole solution of PMMA with spin speed of 5000 rpm on the top of the gate electrode, and then cured at 120 °C for 1 h. Pentacene was thermally evaporated through a shadow mask, as the organic semiconductor, to a thickness of 50 nm at a deposition rate of 0.03 nm s⁻¹. Then, after seven days, a 50 nm gold layer was deposited through a shadow mask by thermal evaporation as source and drain top contacts. Double sweep current (*I*) versus voltage (*V*) characteristics of the transistors were recorded at room temperature (21 ± 2 °C) using a Hewlett Packard (HP) 4140B picoammeter. The devices were stored under vacuum at room temperature between measurements to reduce the effects of atmospheric degradation.

3. Results and discussion

In order to optimise the fabrication process, source and drain Au contacts were evaporated directly after the evaporation of pentacene for some OTFTs, while other devices left under vacuum for seven days before the evaporation of Au electrodes. Atomic force microscopy (AFM) images were used during this investigation to extract the morphology of the deposited Au electrodes for both sets of devices. The surface morphology of 50 nm gold contacts grown on 50 nm pentacene film varied significantly for the two fabrication processes, as shown in Fig. 2, where image (a) represents Au electrodes evaporated after seven days (Device A) and image (b) represents Au electrode evaporated directly after the evaporation of pentacene (Device B). Uniform, crack-free and pinhole-free film is observed when the gold contacts were deposited after seven days,

as shown in Fig. 2(a). In contrast, surface defects were observed when Au electrodes deposited directly after the evaporation of pentacene, as shown in Fig. 2(b). As the same pentacene deposition process and thickness were used for both sets of devices, the difference in Au morphology is attributed to the time used to allow pentacene film to homogenise before the evaporation of Au electrodes.

The impact of pentacene films homogeneity and the period pentacene stored before gold contacts deposition is also clear in the electrical characterisation of OTFTs. Fig. 3(a) and (c) shows plots of typical output characteristics representing the dependence of drain–source current (*I*_{DS}) on the drain–source voltage (*V*_{DS}) of a p-type OTFT devices; the gate bias varied in the range 0 to –25 V with step size of 2.5 V and 0 to –85 V with step size of 5 V for devices A and B, as shown in Fig. 3(a) and (c) respectively. The transfer characteristic which represents the dependence of *I*_{DS} on the gate–source voltage (*V*_{GS}) of the organic transistor are shown in Fig. 3(b) and (d) for *V*_{DS} = –30 and –80 V, for devices A and B, respectively. Plots are given in the form of both (*I*_{DS})^{1/2} versus *V*_{GS} and log(*I*_{DS}) versus *V*_{GS}. The channel width (*W*) is 1000 μm and the channel lengths (*L*) are 95 and 145 μm, for devices A and B, respectively. The field-effect mobility, *μ*, of the devices was estimated from:

$$I_{DS} = \frac{\mu W C_i}{2L} (V_{GS} - V_T)^2 \quad (1)$$

where *C_i* is the insulator capacitance per unit area and *V_T* is the threshold voltage. The threshold voltage represents the value of *V*_{GS} at which the transistor is turned on and can be determined from the intercept of the plot of (*I*_{DS})^{1/2} versus *V*_{GS}. In addition, from Fig. 3(b) and (d), the plot of *I*_{DS(sat)} on a logarithmic scale versus *V*_{GS} (blue curve) is used to evaluate the ratio between the on-current and off-current (on/off current ratio), which is denote for the switching performance of the TFTs. It is clear from Fig. 3 that optimised devices show improved parameters of on-off ratio of 4.1 × 10⁴ and *μ* of about 1.32 cm² V⁻¹ s⁻¹ as well as negligible gate leakage current. On the other hand, devices with Au contacts evaporated directly after the deposition of pentacene show large leakage current with on-off ratio of 1.5 × 10² and *μ* = 0.6 × 10⁻³ cm² V⁻¹ s⁻¹ as well as very high operating voltage. The clear drain off-set current in Fig. 3(c) (negative *I*_{DS} values at *V*_{DS} = 0 V) is indicative of a large leakage gate current. The cause of this leakage current is believed to be due to the pin-holes in the spin-coated insulator. However, optimised devices, Fig. 3(a), show almost no leakage current as the interface between the insulator and the semiconductor

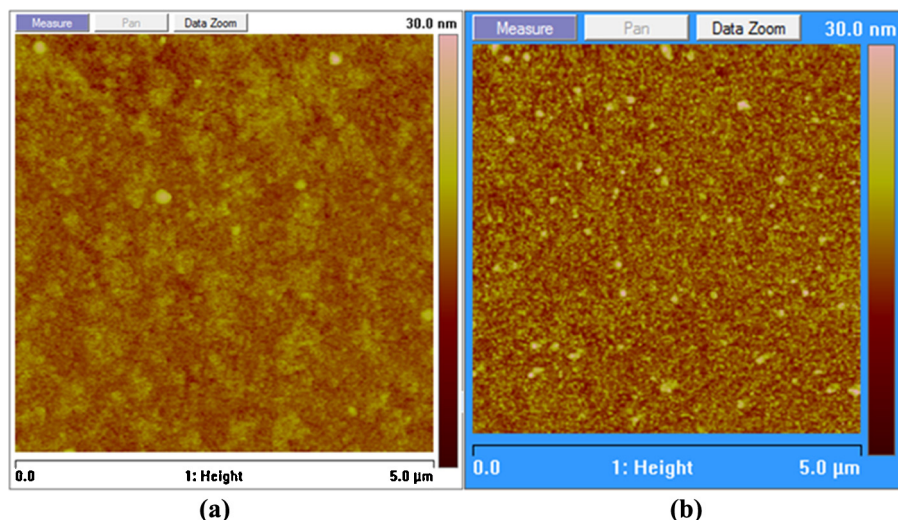


Fig. 2. AFM images of 50 nm gold contacts deposited on 50 nm pentacene, (a) deposited after seven days of the deposition of pentacene, and (b) directly evaporated after the evaporation of pentacene.

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