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Dynamic charge transport in pentacene and zinc oxide thin-film transistors: Dark and UV illumination conditions

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ABSTRACT

The electronic charge transport of thin film transistors (TFTs) based on pentacene and zinc oxide semiconductors was studied. A mathematical model is presented based on the variable range hopping (VRH) transport theory. Using the VRH model, the expression of source drain current is established under dark and under UV illumination (365 nm) in linear regime for drain bias $V_D = -2$ V and 2 V, when we used pentacene and zinc oxide, respectively, at 300 K. All electrical key parameters of TFTs based on pentacene and zinc oxide were extracted. A good agreement between theoretical model and experimental measurement, transfer characteristics was obtained under dark and UV illumination conditions. Finally, we give a simple small-signal equivalent circuit to the organic and inorganic thin film transistor.

1. Introduction

Metal oxide semiconductors have been investigated due to the their high/low conductivity with high visual transparency and have been widely used in a variety of applications (e.g. antistatic coatings, touch display panels, solar cells, flat panel displays, heaters, defrosters, optical coatings, among others) for more than a half-century. One of them is zinc oxide (ZnO) which is a wide band gap transparent semiconductor with excellent chemical and thermal stability and can be deposited on various substrates [1]. Considerable efforts has been made in the development of electronic and optoelectronics devices using this oxide material, in which ultraviolet (UV) light emitting diodes, UV photodetectors, and transparent-field-effect transistor (TFT) [2–5] have been realized. Recently, much attention has been paid on realizing the low-voltage-drive ZnO-TFTs. ZnO is an ideal TFT semiconductor for these applications, having higher field effect mobility than amorphous silicon and lower deposition temperatures than polycrystalline silicon. On the other hand, in recent years organic semiconductors have been extensively studied for various applications in ubiquitous low cost electronics such as solar cells, sensors [6–8], light-emitting diodes, and organic thin-film transistors (OTFTs) [9,10]. In particular, pentacene is a promising organic semiconductor and it has been used as the channel of organic thin film transistors (OTFTs) [11–15]. It exhibits a considerably high field-effect mobility of more than 1 cm^2/Vs [15–24]. Gate-voltage dependent mobility is now a well-recognized feature in organic thin-film transistors (OFETs) [25–31]. Most usually, mobility is found to increase with gate voltage. There are two useful models to account this, which, are the multiple trapping and release (MTR) and variable range hopping (VRH). The basic assumption of MTR [32–34] is a distribution of states localized in the energy gap close to the transport band edge. These states are liable to trap the charge carriers injected into the channel of the transistor, thus reducing the current. When increasing the gate voltage, the Fermi level moves towards band edge as more of the empty traps are filled by injected charge. Accordingly, the ratio of the free to trapped carriers increases, and so does the channel conductivity, which is interpreted in term of an increase of the effective mobility. The VRH model [27] also assumes a distribution of localized levels; it proposes that transport occurs via hopping in that distribution.

In present study, we have studied two types of transistors based on organic material (pentacene) and inorganic material (zinc oxide) under dark and UV illuminations. Using the VRH model, we have extracted the different parameters of the TFTs from the transfer

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characteristics. Finally, we have developed a dynamic model to give a Small-signal equivalent circuit for TFTs.

2. Experimental details

2.1. Preparation of zinc oxide thin film transistor

The zinc oxide film was synthesized by sol–gel method. The zinc acetate hexahydrate ($Zn(CH_3COO)_2{\cdot}2H_2O$), 2-metoxyethanol and monoethanolamine (MEA) were used to prepare ZnO film. For the preparation of nanofibers-ZnO film, equal concentrations of monoethanoamine and Zn^{2+} were used. The precursor solution was mixed with a magnetic stirrer for 2 h in 60 °C and then placed in air for 24 h resulting in a clear and homogeneous sol. p-Silicon with (1 0 0) orientation and thickness of 0.5 mm used in this study was purchased from Sigma–Aldrich company. The Si substrate was cleaned by acetone, methanol, and de-ionized water in ultrasonic bath, respectively. The SiO_2 layer of 200 nm was grown on p-Si substrate in a furnace at 1000 °C for 2 h and it was used as the gate-insulator. The ZnO film of 100 nm was deposited on SiO_2 layer. The thicknesses of the SiO_2 and ZnO layers were determined by a Park System XE-100E atomic force microscopy (AFM). The source and drain electrodes were prepared by evaporating of a 100 nm Al layer through a shadow mask in the form of a top contact geometry. The channel width and length of the transistor are 2500 μm and 100 μm, respectively. The morphology properties of the ZnO film were investigated by a Park System XE-100E atomic force microscopy (AFM). Electrical characteristics are measured by KEITHLEY 4200 semiconductor parameter analyzer. The photoresponse properties of the transistor were performed using a 500 W tungsten lamp.

2.2. Preparation of pentacene thin film transistor

p-Type silicon with (1 0 0) orientation and thickness of 0.5 mm used in this study was purchased from Sigma–Aldrich company. The Si substrate is cleaned by acetone, methanol, and de-ionized water in ultrasonic bath, respectively. The SiO_2 layer of 200 nm was growth on p-Si substrate in a furnace at 1000 °C for 2 h and it was used as the gate-insulator. The pentacene organic semiconductor was purchased from Sigma–Aldrich Company. The pentacene organic layer of 100 nm was thermally evaporated on SiO_2 layer. The thicknesses of the SiO_2 and pentacene organic layers were determined by a Park System XE-100E atomic force microscopy (AFM). After evaporation, the source and drain electrodes were prepared by evaporating of a 150 nm thick Au layer through a shadow mask in the form of a top contact geometry. The channel width and length of the transistor are 2500 μm and 100 μm, respectively. Fig. 1 shows a schematic view of field effect transistor based on pentacene and based on zinc oxide.

3. Model of charge transport

In this paper, we develop model for charge transport in the active layer of organic and inorganic thin film transistors. This charge transport mechanism is based on the variable range hopping VRH theory [35] i.e., thermally activated tunneling of carriers between localized states. In VRH model a carrier may either hop over a small distance with a high activation energy or hop over a long distance with a low activation energy. In TFTs, an applied gate voltage gives rise to the accumulation of charge in the region of the semiconducting layer that is close to the insulator. As these accumulated charge carriers fill the lower-lying states of the organic semiconductor, any additional charges in the accumulation layer will occupy states at relatively high energies. This results in a higher mobility with

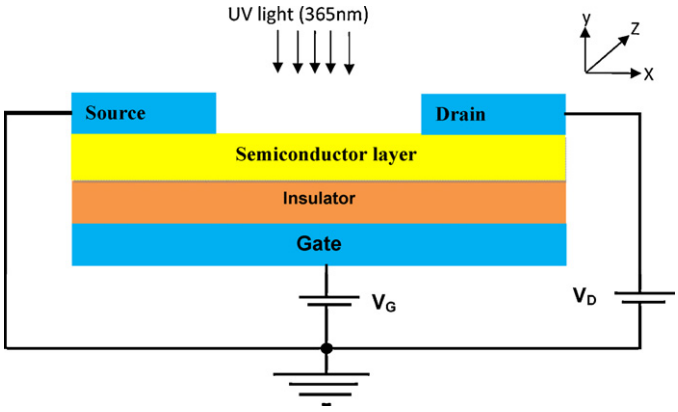

Fig. 1. Schematic of thin film transistors (TFTs).

increasing gate voltage. The influence of temperature and the influence of the filling of states on the conductivity is studied in a VRH system with an exponential distribution of localized-state energies [36]. The temperature dependence of the carrier transport in such a system is strongly dependent on the density of localized states. The source-drain current must be calculated over the entire accumulation channel using the following expression:

$$I_{ds} = \frac{Z}{L}\int_{V_s}^{V_D}\int_{0}^{d}\sigma\left(\delta, T, V\right)\, dydV_c \tag{1}$$

where V_c is the electrostatic and channel potential, d is the organic semiconductor thickness, L and Z are the channel width and length respectively, V_s and V_D are the source and drain voltages respectively and y are the direction perpendicular to the oxide semiconductor interface. The transport of carriers is governed by the hopping of carriers between localized states which is strongly dependent on the hopping distances as well as a resistor network [37,38]. Based on percolation theory [39] an expression is derived for the conductivity σ as a function of the temperature T by [35]:

$$\sigma = \sigma_0\left[\frac{n_s\delta_0(T_a/T)^4\sin(\pi T/T_a)}{(2\alpha)^3 B_c}\right]^{T_a/T}\exp\left[\frac{q(V-V_c)}{K_B T_a}\right]^{T_a/T} \tag{2}$$

where σ_0 is the percolation prefactor, T_a is an effective temperature, B_c is a critical number for the percolation onset which is ≈2.8 for three dimensional amorphous systems, α is the effective wave functions overlap parameter between localized states, q is the elemental charge, n_s the number of localized states per unit volume (density), V the electrostatic potential and δ_0 is the carrier occupation far from the semiconductor–insulator interface ($V=0$) is given by Eq. (3):

$$\delta_0 = \exp\left(\frac{E_f}{K_B T_a}\right)\frac{\pi T}{T_a\,\sin(\pi T/T_a)} \tag{3}$$

where E_f is the Fermi level. The variations of $V(y)$ and $\delta(y)$ with the distance y are determined by the Poisson equation. For the accumulation layer, where $\delta(y) \gg \delta_0$, the relationship between the electrical field and the electrostatic potential is given by:

$$F_y(x,y) = -\frac{\partial V}{\partial y} \tag{4}$$

Changing the integration variable in Eq. (1) from dy and dV the integral expression of the drain current turns out to be:

$$I_{ds} = \frac{Z}{L}\int_{V_s}^{V_D}\int_{V_s}^{0}\frac{\sigma(V,V_c)}{-F_y}\,dVdV_c \tag{5}$$

In order to evaluate the integral on the right hand side of Eq. (5) an expression of σ/F_y in the accumulation layer should be defined