Synthetic Metals 160 (2010) 83–87

Contents lists available at ScienceDirect

Synthetic Metals

journal homepage: www.elsevier.com/locate/synmet

N-channel operation of pentacene thin-film transistors with ultrathin polymer gate buffer layer

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ARTICLE INFO

Article history:
Received 17 April 2009
Received in revised form
24 September 2009
Accepted 5 October 2009
Available online 4 November 2009

Keywords:
Gate buffer layer
Electron trap
Ambipolar transport
Organic thin-film transistor
Pentacene

ABSTRACT

N-channel operation of pentacene thin-film transistors with ultrathin poly(methyl methacrylate) (PMMA) gate buffer layer and gold source–drain electrode was observed. We prepared pentacene thin-film transistors with an 8-nm thick PMMA buffer layer on SiO_2 gate insulators and obtained electron and hole field-effect mobilities of 5.3×10^{-2} cm^2/(V s) and 0.21 cm^2/(V s), respectively, in a vacuum of 0.1 Pa. In spite of using gold electrodes with a high work function, the electron mobility was considerably improved in comparison with previous studies, because the ultrathin PMMA film could decrease electron traps on SiO_2 surfaces, and enhance the electron accumulation by applied gate voltages.

1. Introduction

Control of the conduction type in organic thin-film transistors (OTFTs) is one of the most important issues to be solved for realizing their practical application such as organic complementary circuits (CMOS) and light emitting devices [1]. It is well known that a large part of π-conjugated molecules are so-called *p*-type semiconductors in air, although newly synthesized molecules with a small bandgap [2] or high electron affinity [3] can be employed as *n*-type even in air. However, the carrier transport in organic devices is greatly influenced by several outer factors. For example, the type of majority carrier depends on the degree of vacuum and the kind of gas atmosphere [4]. Moreover, the electron injection from metal electrodes with low work functions (e.g., aluminum and calcium) into organic semiconductor layers causes *n*-channel conduction even in transistors based on *p*-type semiconductors [5,6]. Recently, many single-component *p*-channel OTFTs were driven in *n*-channel operation by utilizing polymer gate dielectrics [7–9] and inserting polymer layers into semiconductor/oxide-insulator interfaces [10–13].

Even pentacene thin-film transistors, which are well known for its large hole field-effect mobility (∼1 cm^2/(V s)), were reported to show *n*-channel operation with various methods described above [5–8,10,13]. However, the electron field-effect mobility of pentacene transistors reported in previous works was still much smaller than the hole mobility. It has been theoretically suggested that organic semiconductors, in general, can be good transport materials for both electron and hole [14]. The achievement of high mobility for both electron and hole has been strongly required in terms of both industrial and academic viewpoints, e.g. for realizing high-performance, low-cost CMOS with OTFTs, and for understanding the carrier injection/transport mechanism in organic semiconducting devices.

Here, we demonstrated *n*-channel operation of pentacene TFTs with gold (Au) source–drain electrode, by depositing an 8-nm thick poly(methyl methacrylate) (PMMA) film onto a SiO_2 gate dielectric. In our previous works, the increase of the electron mobility for *n*-channel OTFTs based on *N,N′*-ditridecyl-3,4,9,10-perylenetetracarboxylic diimide (PTCDI-C13) [15] and 1,4,5,8-naphthalene tetracarboxylic dianhydride (NTCDA) [16] was observed by utilizing this ultrathin PMMA gate buffer layer, although electron injection barrier between a work function of Au electrode (5.1 eV) and LUMO (lowest unoccupied molecular orbital) of *n*-type semiconductors (PTCDI-C13 (4.0 eV) [3] and NTCDA (3.6 eV) [17]) was expected to be large. Similar to the study on these *n*-channel transistors, a high electron field-effect mobility (5.3×10^{-2} cm^2/(V s)) for pentacene TFTs was also obtained in this work despite a large electron injection barrier between Au electrode and LUMO of pentacene (3.2 eV) (Fig. 1(a)) [5]. The influence of the PMMA spacer

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doi:10.1016/j.synthmet.2009.10.009

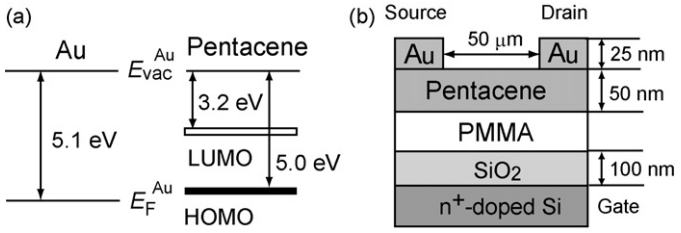

Fig. 1. (a) Energy band diagrams of an Au electrode and pentacene. (b) Structure of a pentacene TFT with a PMMA buffer layer.

on *n*-channel operation of pentacene transistors was considered.

2. Experimental procedure

Pentacene and PMMA were purchased from Aldrich. A PMMA layer was deposited by spin-coating onto a thermally grown SiO_2 on heavily doped *n*-type silicon wafer. The nominal thickness of the SiO_2 layer was 100 nm. The details of preparation of the PMMA film were described elsewhere [15,16,18]. The X-ray reflectivity (XR) measurement for the ultrathin PMMA film was performed with a commercial measurement system (ATX-G, Rigaku) using Cu K_α radiation. The XR profiles were analyzed with a Rigaku GXRR data-fitting software based on the theory of Parratt [19]. Ellipsometric measurements were performed for PMMA films thicker than 100 nm, using a DHA-FX (Mizojiri Optical Ltd.).

Pentacene was purified by sublimation twice and thermally evaporated onto SiO_2 coated with PMMA under a pressure of 1.0×10^{-4} Pa. The thickness of pentacene films and the substrate temperature were set to be 50 nm and 338 K, respectively. Successively, the pentacene film specimens were transferred into another metal deposition chamber with a short air exposure for 10 min, and 25-nm thick Au source–drain electrode with the channel length (L) of 50 μm and width (W) of 1 mm was deposited onto the pentacene films. Thus, top-contact transistors were fabricated as shown in Fig. 1(b).

The prepared TFTs were taken out from the evaporation chamber and put into a vacuum probe system (ST-500, JANIS) within 10 min after this temporary air exposure of specimens. Then, transistor characteristics were measured in a vacuum (0.1 Pa), with a Keithley 4200-SCS semiconductor parameter analyzer. The field-effect mobility for electron (μ_e) and hole (μ_h) and threshold voltage (V_T) were calculated from transfer characteristics (drain–source saturation current ($I_{D,sat}$) vs. gate voltage (V_G)) according to the following equation:

$$I_{D,sat} = \frac{WC_i\mu_{e(h)}(V_G - V_T)^2}{2L}, \quad (1)$$

where C_i is the gate capacitance. Here C_i was determined by an LCR meter (HP4263A, Agilent) at a frequency of 100 Hz, by using a stacking structure of PMMA, SiO_2 and a heavily doped Si substrate, on which upper Au electrodes were deposited by vacuum evaporation. The measured C_i values for the PMMA/SiO_2 layers employed in this work were smaller than the measured value for the SiO_2 film (30.7 nF/cm^2), confirming that unintended increase of C_i due to the existence of PMMA did not occur.

The surface morphology of pentacene films was observed with an atomic force microscope (AFM) (JSPM-5200, JEOL) and the crystal structure was examined using an X-ray diffractometer (XRD) (MXP^3, BrukerAXS) with Cu K_α radiation.

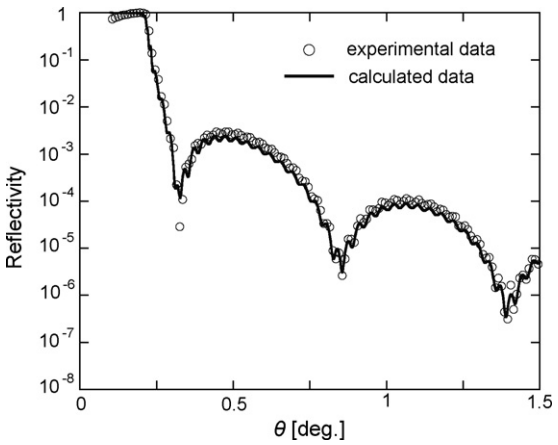

Fig. 2. X-ray reflectivity profile for the ultrathin PMMA film prepared onto a SiO_2/Si substrate. The black solid line is the curve best-fitted for the experimental result (open circles).

3. Experimental results

3.1. Characterization of the ultrathin PMMA layer and pentacene thin films

A result of XR measurement for the stacking structure of PMMA, SiO_2 layers and a Si substrate was shown in Fig. 2. An interference fringe (Kiessig fringe) owing to the ultrathin PMMA layer was observed clearly. From the best-fitted curve for the experimental result, the thickness of 8.0 nm, the density of 1.19 g/cm^3, and the surface roughness of 0.33 nm were estimated for the PMMA film, respectively. And the thickness of the SiO_2 layer was calculated to be 106.3 nm at the same time. This result suggests that PMMA was deposited uniformly over the whole surface of SiO_2, since the surface roughness was very small and the density was the same as that of bulk PMMA (1.19 g/cm^3). The capacitance of the double layer of this 8-nm thick PMMA and SiO_2 was measured to be 29.3 nF/cm^2.

Fig. 3 shows AFM images and XRD profile of pentacene thin films. For comparison, the surface morphology of pentacene films prepared on a bare SiO_2 under the same evaporation condition was also shown there. In our experiment, the grain size of pentacene films on PMMA was on average smaller than that of films on SiO_2. Recently, the surface morphology of pentacene on various polymer dielectrics such as poly(4-vinylphenol) (PVP) [8], poly(vinyl alcohol) (PVA) [8,20], and PMMA [20], has been discussed in terms of the surface energy, and it was reported that PMMA layer promotes grain growth of pentacene [20]. However, we could not observe such an effect in this work. The pentacene film on PMMA showed sharp X-ray diffraction peaks of (0 0 l) (l = 1–5) reflection of a thin-film phase, accompanied with smaller peaks of (0 0 m) (m = 1–4) reflection of a bulk phase [21]. The larger ratio of the thin-film phase in pentacene films can lead to the higher field-effect mobility because it is thought that π-overlap in the plane of the substrate in the thin-film phase is greater than in the bulk phase [21]. Therefore, good carrier transport between source and drain electrodes was expected in this pentacene film on the PMMA spacer.

3.2. Characterization of the pentacene TFT with the ultrathin PMMA layer

Fig. 4 presents output characteristics (drain–source current (I_D) vs. drain–source voltage (V_D)) of pentacene TFTs with the 8-nm thick PMMA layer. The device displayed a typical *p*-channel operation for negative V_D and V_G as shown in Fig. 4(a). In the configuration of *n*-channel operation (positive V_D and V_G), the drastic increase of