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Response of as grown dislocation structure to temperature and stress treatment in multi-crystalline silicon

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Abstract—Dislocations and dislocation networks in multi-crystalline (mc) silicon wafers for photovoltaic applications act as minority carrier recombination centers and thus limit the efficiency of solar cells. The literature shows results for a massive dislocation reduction by applying an annealing procedure in combination with and without an impurity gettering step. In this work different kinds of annealing experiments with mc silicon samples were carried out at 1200 °C and 1365 °C for 1 h to 96 h under an applied stress of up to 4.2 MPa under pure inert or boron containing atmospheres. The results show clearly that, under the used process conditions, a dislocation reduction could not be observed via defect selective etching using different kinds of etchants. It was found, that it is essential to carefully select the etching solution as the electrical resistivity of the samples might change after a respective thermal treatment, such that the eventually still present dislocations will not be overseen. © 2015 Acta Materialia Inc. Published by Elsevier Ltd. All rights reserved.

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1. Introduction

Dislocations and dislocation networks in multi-crystalline (mc) silicon wafers for photovoltaic applications act as minority carrier recombination centers [1–4] and thus limit the efficiency of solar cells. In order to mitigate the influence of dislocations on the efficiency of mc silicon solar cells a dislocation density below 10^4 cm⁻² is necessary [5]. On the one hand this requirement led to the development of new crystallization techniques for growing silicon crystals for photovoltaic applications with a reduced dislocation density, like the so-called dendritic casting technique [6,7], the growth of mc silicon ingots with fine grain structure (also called high performance multi) [8,9], growth of quasi-mono or mono-like silicon [10–14] or the float cast method [15].

On the other hand several publications suggest that alternative approaches may be effective in order to reduce the dislocation density of as-grown silicon after the crystallization process. In each of these cases bulk samples or wafers, which were prepared from silicon ingots or ribbons were thermally treated by just using either an additional annealing step [16,17], a boron- and phosphorus-diffusion gettering procedure at elevated temperatures [18] or a combined stress and temperature treatment [19]. It was reported that a reduction of the dislocation density of up to 95% is possible by using such procedures [16]. This would imply that the mc silicon material could exhibit a final dislocation density of only 5×10^2 cm⁻² to 5×10^4 cm⁻² in comparison to an initial dislocation density of 1×10^4 cm⁻² up to 1×10^6 cm⁻² [16].

In order to proof the findings reported in the literature, a detailed and systematic experimental analysis was carried out to investigate the response of the as-grown dislocation structure in mc silicon samples subjected to an annealing treatment with and without applied mechanical stress and furthermore with regard to a long term boron diffusion gettering experiment. For that purpose the dislocation structure in the samples before and after thermal treatment was analyzed by defect selective etching (DSE).

2. Experimental methods

Two different types of annealing experiments were carried out. In the case of experimental series A, a mechanical stress was additionally applied (see Section 2.2.1), while in experimental series B, extremely long annealing times were used, partially in combination with different environmental conditions (see Section 2.2.2).

2.1. Description of the samples and the characterization methods

For the experiments mc silicon samples, boron doped, with an electrical resistivity of around 1.6–1.8 $\Omega\,cm$ were

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Fig. 1. Process flow which was used to process and characterize the silicon samples (a). Parameters used for experiment series A (time, temperature and mechanical load) (b).

Table 1. Composition and properties of the Secco, Schimmel, and Sopori etching solutions.

Etching solution	Secco	Schimmel	Schimmel (diluted)	Sopori
Composition	2 (HF 49%): 1 (0.15 M	2 (HF 49%):	2 (HF 49%): 1	36 (HF 49%): 15 (CH ₃ COOH):
	K ₂ Cr ₂ O ₇ solution)	1 (1 M CrO ₃)	(1 M CrO ₃): 1.5 (H ₂ O)	2 (HNO ₃ 70%)
Proportion Oxidant/Complexing agent	0.003	0.018	0.018	0.033
Bulk etch rate [μm/min]	1.5	2	2	20
Applicable resistivity range [Ωcm]	4–300	4–15	0.01	?

used. They were prepared from the middle part of a silicon ingot stemming from industrial production (experiments A) and from one crystal grown in a laboratory scale furnace (experiments B1-B5). The samples had a size of 50 mm × 50 mm and a thickness of 750 µm in the case of experimental series A and a size of 13 mm × 13 mm and a thickness of 600 µm in the case of experimental series B.

Fig. 1 shows the typical work flow which was used to process and characterize the samples. After the initial preparation of the samples they were polished on both faces with diamond suspensions with a grain size of 9 μ m, 3 μ m, 1 μ m, and a finishing step with silicon dioxide suspension with a grain size of 50 nm. Subsequent cleaning of the samples was done with ultrasonic agitation in acetone, 2-propanol and deionized water.

For defect selective etching (DSE) three different etching solutions were evaluated: Secco [20], Schimmel [21] and Sopori [22]. Table 1 gives an overview over the compositions and the properties of the three different etching solutions.

All three solutions use HF as a complexing agent, while the oxidant either is $K_2Cr_2O_7$ in the Secco solution, CrO_3 in the Schimmel solution, and HNO₃ in the Sopori solution. The proportion of the oxidant to the complexing agent defines the selectivity of the etchant toward defects. With a low concentration of the oxidant only parts of the sample surface which contain decorated crystal defects can be etched. With raising the oxidant concentration the bulk etch rate increases, while the defect selectivity decreases. With increasing doping level, respectively with decreasing electrical resistivity, the bulk etch rate of the sample rises, too. Therefore, a special formulation of the Schimmel solution exists for samples with a low electrical resistivity. Because of these considerations the Secco solution was chosen as the standard defect selective etching solution since the samples had a resistivity of around $1.6-1.8 \Omega$ cm. In some cases the diluted Schimmel etchant was used for instance when a decrease of the resistivity of the samples was observed after the thermal treatment (see Section 3.2.2). All etching experiments were carried out at room temperature under agitation by a magnetic stirrer. An etching time of five minutes was used for the Secco solution and 20 min for the diluted Schimmel etchant. These etching times have been determined in separate experiments to be well suited for the different resistivity ranges.

After the DSE procedure the initial etch pit density on the full area of the samples was analyzed under an optical microscope. In all samples the dislocation density was non-uniform and typically varied from 10^4 cm^{-2} up to 10^6 cm^{-2} with an average value of around 10^5 cm^{-2} .

Subsequent to this analysis, a polishing step was carried out by using only 3 μ m, 1 μ m and silicon dioxide suspensions. This results in a removal of approximately 20 μ m material thickness. Then, samples were cleaned, thermally treated (see Section 2.2), polished by using the same procedure as after the first DSE step, defect selectively etched and analyzed again under the microscope in order to determine the etch pit density after the thermal treatment.

2.2. Description of the annealing experiments

2.2.1. Experimental series A

The first type of experiment (Experimental series A) made use of a three-line-bending configuration as shown in Fig. 2(a). The squared mc silicon sample rested on two graphite beams and was loaded in the middle by a graphite

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