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Future directions for higher-efficiency HIT solar cells using a Thin Silicon Wafer

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ABSTRACT

To reduce the power generation cost of heterojunction with intrinsic thin layer (HIT) solar cells, it is necessary to use a thinner crystalline silicon wafer, as well as to improve the conversion efficiency. We have experimentally confirmed that V_{OC} of the HIT solar cell increases with decreasing the wafer thickness, and can reach a very high V_{OC} of 747 mV with a 58-μm-thick wafer owing to a sufficiently low surface recombination velocity. We also indicate the future directions for improving the efficiency. The uniformization of the texture size of the silicon surface and reduction of the carrier density in TCO film while maintaining an equal or lower conductivity are effective for improving the optical confinement.

1. Introduction

The global demand for solar energy has been increasing. The world production volume of solar cells exceeded 23 GW in 2010, and is expected to continue growing in the future. Since commercializing the HIT solar cell in 1997, we have steadily expanded its production. Moreover, we plan to increase the production capacity from 600 MW in FY 2010 to 1.5 GW by FY 2015.

The power generation cost is the most important parameter for the customer. Despite considerable effort to reduce the production cost, however, the power generation cost of solar cells is still much higher than those of other power generation methods. So that PV device can become a major power source, we must considerably reduce the power generation cost of solar cells. One of the most effective approaches for reducing the production cost is to reduce the amount of material used. In particular, bulk silicon substrates account for about 40% of the total production cost of typical c-Si-based solar modules [1]. The reduction of the Si wafer thickness is essential. Another is to improve the conversion efficiency, which affects all the costs of the cell, module and installation.

Fig. 1 shows the progress in the conversion efficiency of HIT solar cells at the R&D stage. We achieved excellent conversion efficiency of 23.0% with a practical size of 100.4 cm^2 and 22.8% with a thin c-Si cell of 98 μm in 2009 [2].

2. Structure of HIT solar cell

The structure of the HIT solar cell is shown in Fig. 2. On one surface, a p-type a-Si layer is formed on an i-type a-Si layer deposited on a textured n-type crystalline silicon substrate to form a p-n junction. On the other surface, an n-type a-Si layer is formed on an i-type a-Si layer deposited on the n-type substrate to form a back surface field (BSF) structure. On both sides of the doped a-Si layers, transparent conductive oxide (TCO) and metal grid electrodes are fabricated. All these fabrication processes are conducted below 200 °C to avoid any thermal damage to the cell components.

The most distinctive characteristic of the HIT solar cell is the excellent surface passivation of c-Si achieved by the deposition of a high quality i-type a-Si layer [3,4]. This very thin intrinsic a-Si layer terminates the dangling bonds at the heterointerface and decreases the defect density, which enables not only a very high open-circuit voltage (V_{OC}) of more than 720 mV but also a better temperature coefficient of −0.23%/degree [5]. In addition, the symmetrical structure of the HIT solar cell is suitable for application to a bifacial module [6]. These excellent characteristics of the HIT solar cell can bring considerable benefits to customers because the annual amount of output power is higher from the HIT solar cell than that of other c-Si solar cells with the same nominal output.

We attained the world's top level conversion efficiency of 23.0% in 2009 as shown in Fig. 3 [2]. To gain a more competitive advantage, some of the technologies used to obtain the 23.0% efficiency have been transferred from the R&D stage to mass production. In addition, we have improved the design of our module. To decrease the resistance loss, we have increased the number of tabs without increasing the shadowing loss. Moreover, by adopting an antireflection coating glass, we have successfully produced a new HIT N Series of 240-W models with a high module conversion efficiency of 19.0% and a cell conversion efficiency of 21.6% [7].

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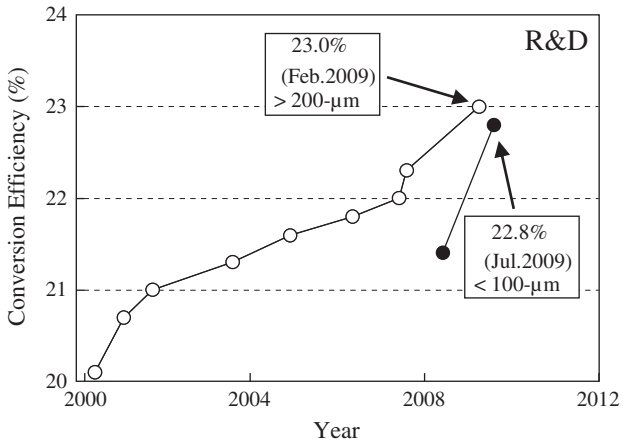

Fig. 1. Progress in the conversion efficiency of HIT solar cells.

To reduce the production cost of HIT solar cells, it is very effective to adopt a thinner Si wafer. However, using a thinner silicon wafer also poses several problems. One is the easy warping of the solar cells, which can decrease the process yield. Another is the drop in photocurrent arising from the short optical path length. Another is the increased impact of surface recombination on the effective lifetime of excess carriers, which has a negative effect on V_{OC}. Our approaches for obtaining high-efficiency HIT solar cells with thinner silicon wafers will be described in the following section.

3. Experimental results

HIT solar cells with various thicknesses were manufactured with using typical fabrication process conditions. Fig. 4(a) shows a photograph of a HIT solar cell of 58 μm thickness. There is no warping. The symmetrical structure of the HIT solar cell and the low-temperature process make it advantageous from the structural and thermal viewpoints.

Fig. 4(b) shows the behavior of PV parameters normalized by the corresponding values for a 96-μm-thick wafer. As expected, I_{SC} decreases with decreasing wafer thickness owing to the reduction of the optical path length. On the other hand, V_{OC} increases as the wafer thickness decreases. A very high V_{OC} of 747 mV was achieved with a 58 μm substrate. Thus, it is confirmed that the drop in I_{SC} with the use of the thinner Si wafer can be compensated owing to the increase in V_{OC} in the HIT solar cell. This characteristic shows that the HIT structure is advantageous for the use of a thinner silicon wafer. The increase in V_{OC} is attributable to the low surface recombination velocity, as described below.

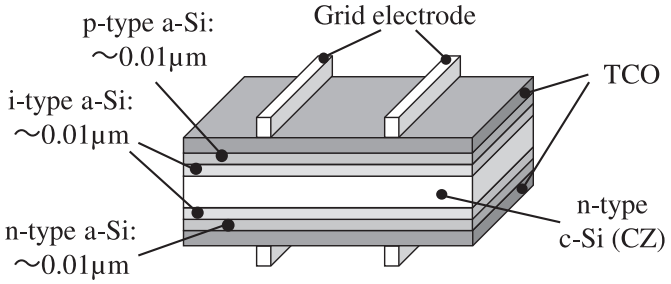

Fig. 2. Schematic illustration of a HIT solar cell.

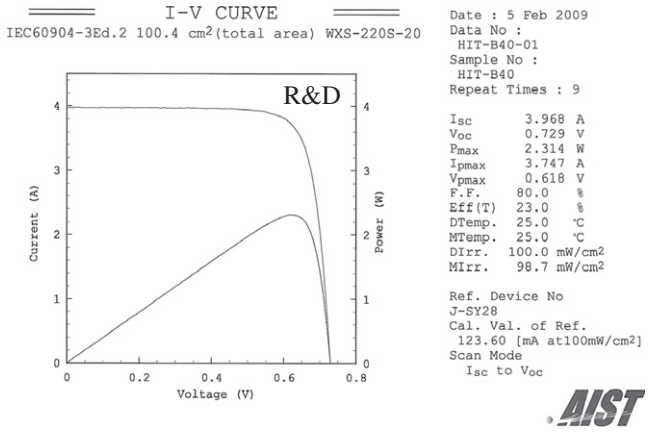

Fig. 3. I–V characteristics of the 23.0% efficiency HIT solar cell.

The effective lifetime of a solar cell can be represented by Eq. (1) [8].

$$\frac{1}{\tau_{eff}} = \frac{2}{W}S + \frac{1}{\tau_{bulk}} \tag{1}$$

Here, τ_{eff} is the effective lifetime, W is the wafer thickness, S is the surface recombination velocity and τ_{bulk} is the bulk lifetime. According to this relationship, the effective lifetime of excess carriers is reduced as the wafer thickness decreases, resulting in a decrease in V_{OC}. Fig. 5(a) shows the correlation between the reciprocal of the effective lifetime and two divided by wafer thickness. A linear relationship can be observed, and the slope of this curve indicates the surface recombination velocity. The surface recombination

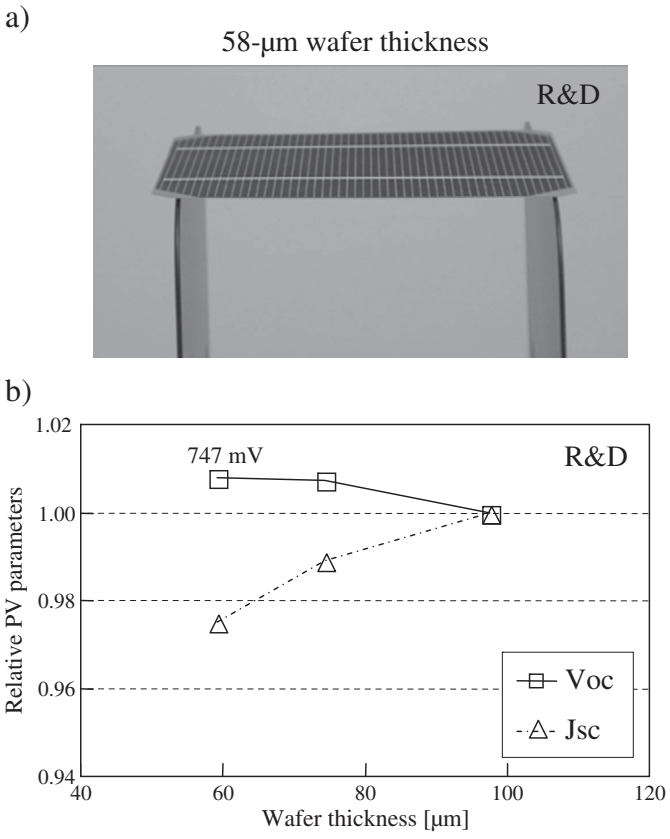

Fig. 4. (a) Photograph of a HIT solar cell with a 58-μm-thick wafer, (b) behavior of parameters for HIT solar cells with a silicon wafer thinner than 100 μm. Values are normalized by these for a solar cell with a 96-μm-thick wafer.