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Influence of textured c-Si surface morphology on the interfacial properties of heterojunction silicon solar cells

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ABSTRACT

For the HIT solar cells, the properties of interface between intrinsic thin film and c-Si are critical for the resulting device. The interfacial properties mainly depend on the surface passivation quality of c-Si, which is found to be affected by the morphology of textured surfaces. In this study, four kinds of textured c-Si substrates are fabricated: large pyramids without chemical polished (CP), large pyramids with CP, small pyramids without CP and small pyramids with CP. We investigated the effects of textured-surface morphology on the passivation of c-Si, the thin layer coverage and the interfacial properties of heterojunction prepared by HWCVD. Minority carrier lifetime measurements show that the wafer with small pyramids leads to better surface passivation than the one with large pyramids. The good coverage and contact between the thin film and the substrate can be achieved and no epitaxial growth occurs on the wafer with small pyramids through the study of TEM. Dark I-V measurements reveal that the heterojunction on wafer with small pyramids and CP has low recombination at the a-Si:H/c-Si interface. Our results indicate that the surface with small pyramids and low surface roughness is beneficial to the performance of HIT solar cells.

1. Introduction

The heterojunction with intrinsic thin-layer (HIT) solar cells are of great interest for the photovoltaic development due to their high-efficiency and low-cost fabrication process [1,2]. Up to now, Sanyo has achieved the world's highest conversion efficiency of 23% for solar cells fabricated by plasma enhanced chemical vapor deposition (PECVD) on an n-type Cz wafer [3]. For HIT solar cells, the interfacial properties between a-Si:H and c-Si make significant influence on the cell's efficiency. Such good passivation of the wafer surfaces becomes critical in making device voltage reach higher value [4]. The quality of surface passivation is mainly determined by the microstructure of a-Si:H layer, which not only depends on the deposited parameters and the deposited technology but also is related to the surface morphology of c-Si [5,6].

Generally, the Si wafers are textured randomly by chemical anisotropic etching with a NaOH or KOH solution, which is the standard process to obtain pyramids with the average size of 8-10μm[7,8]. As an alkaline and strong oxidizing reagent, NaClO can be used to obtain small and uniformed pyramids with the average size of 1–3μmon the Si wafer and to remove organic contaminants on the surface of wafer [9]. It is assumed that the wafer with small and uniformed pyramids owns advantages in HIT cell preparation, because the surface with small roughness is beneficial to improve the coverage and contact between the thin layers and substrate, which is helpful to increase the open voltage and fill factor of solar cells [10]. However, the good passivation of Si wafer is regularly more cumbersome to be realized on the textured surface, and it is likely due to the presence of localized recombinative paths situated at the pyramid valleys [11]. Thus, in order to obtain the higher-efficiency cell on textured substrate, we have to avoid the appearance of the epitaxial growth and guarantee the good contact between the thin layers and substrate, also the perfectly performed passivation on textured surface is necessary. Here, we presented that this issue may be resolved by selecting silicon substrate morphology and fabricating the heterojunction by HWCVD.

In this paper, we prepared the Si heterojunction by HWCVD and studied the effects of the textured-surface morphology on the thin layer coverage, the passivation of c-Si and the interfacial properties of heterojunction. Minority carrier lifetime has been measured after the H treatment and deposition of a-Si intrinsic layer in order to study the passivation effect. The microstructure of i-layer and the contact between i-layer and the substrate were studied through TEM. Dark I-V measurements were conducted to analyze the interfacial properties of heterojunction with the structure of Al/(n)a-Si:H/(i) a-Si:H/(p)c-Si/Al.

2. Experimental details

The c-Si substrates (CZ, P-type, 1-10 Ω cm) with (100) surface orientation were used. First, to eliminate the native oxide on the surface, the wafer was treated in 2% HF solution for 60 s before the saw damage removing and texturation. The saw damage was removed in a 20 wt% NaOH solution at 80 °C for 10 min. Then the samples were

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Table 1
Conditions for NaOH and NaClO texturizaiton.

Sample	Solution	Concentration	Additives	Temperature and Time	CP
Large	NaOH	3 wt.%	1wt%Na_2SiO_3 + 7vol%IPA	80 °C 50 min	–
Large + CP	NaOH	3 wt.%	1wt%Na_2SiO_3 + 7vol%IPA	80 °C 50 min	HNO_3 + CH3COOH + HF
Small	NaClO	Available Chlorine 9%	15 V%C_2H_5OH	80 °C 80 min	–
Small + CP	NaClO	Available Chlorine 9%	15 V%C_2H_5OH	80 °C 80 min	HNO_3 + CH3COOH + HF

Table 2
Deposition conditions for the thin films.

	T_s(°C)	T_f(°C)	H2(sccm)	SiH4(sccm)	PH5(sccm)	Pressure(Pa)	Time(s)
H treatment	25	1850	20	–	–	10	30
(i)a-Si:H	25	1780	3	1	–	1	15
(n)a-Si:H	25	1780	3	1	0.01	2	42

textured with the solution of NaClO and NaOH, respectively. The texturing parameters are listed in Table 1. CP etching was carried on in the solution consisted of HNO3: CH3COOH: CH3COOH = 6:3:1 for 4 min. All the wafers were cleaned by the standard RCA process to remove organic and metallic contaminants from the c-Si surface. The oxide removal in HF is performed before amorphous layer deposition by HWCVD. The deposition parameters are listed in Table 2. Atomic hydrogen treatment for the c-Si surface was done before depositing the films. The minority carrier lifetime was measured by a WT-2000 wafer scanner. The coverage and contact between the thin film and the substrate was studied by TEM, and the dark I-V characteristics of the heterojunction were obtained at 300 K.

3. Results

We fabricated various textured morphologies obtained by NaClO and NaOH solutions, as shown by the scanning electron microscopy (SEM) micrographs in Fig. 1, from (a) small ones (1–3 μm) to (b) large ones (8–10 μm). After pyramid formation, CP was adopted to reduce the sharpness of pyramids. It results in a pyramid rounding, with small surface roughness, as presented in Fig. 1(c) and (d). With the CP time (t_{CP}) increased from 0 to 4 min, the average angle of pyramid peak (φ) increased from 73.8° to 110.6° for the sample textured by NaClO, and φ increased from 73.7° to 101.8° for that one textured by NaOH.

The passivation of the c-Si surface by intrinsic a-Si:H layers with the thickness of 50 nm deposited on both sides of c-Si is studied by minority carrier lifetime (τ) measurements. We present the results in Fig. 2 with error bars obtained based on possible error in measurements. Fig. 2 shows that the value of τ is smallest for the sample with large pyramids without CP, whereas the value of τ is largest for the sample with small pyramids and CP. The values of τ for the sample with small pyramids without CP and the sample with large pyramids with CP is almost the same.

The cross-sectional TEM images of the a-Si:H layer with the thickness of about 20 nm deposited on the surface of c-Si textured by NaClO are shown in Fig. 3. It is seen that the a-Si:H layer covers the

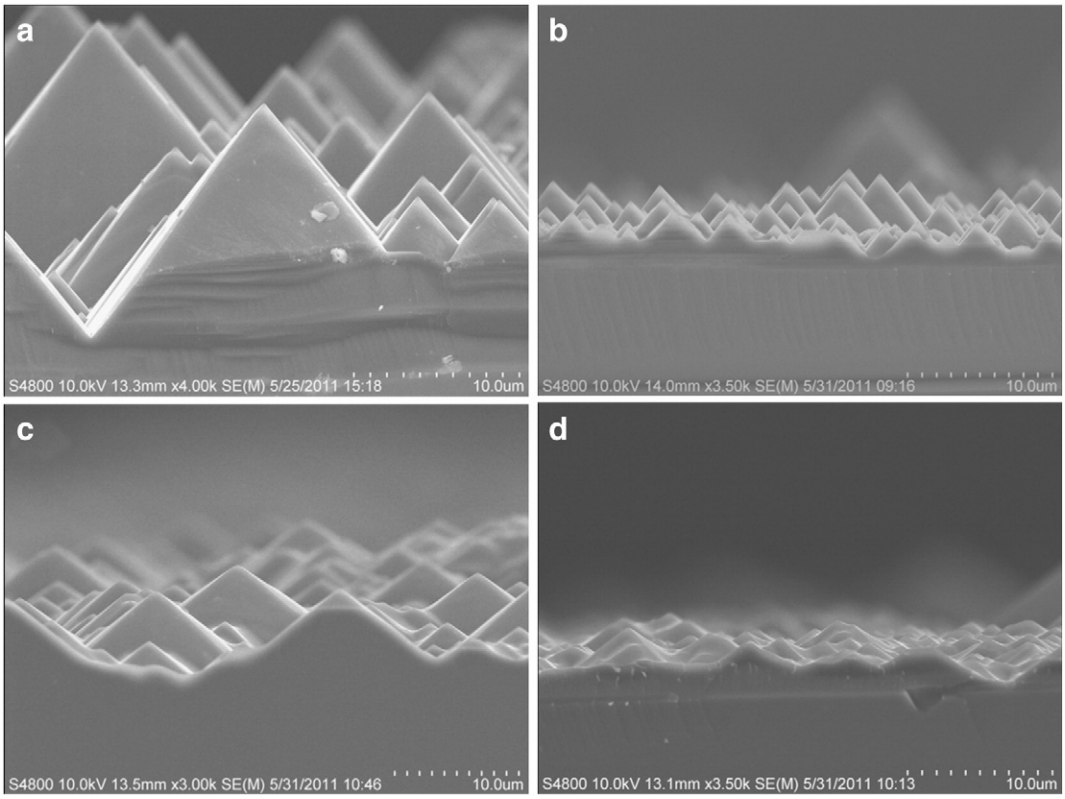

Fig. 1. SEM photographs of c-Si with different sizes and shapes of pyramids, (a) large pyramids, (b) small pyramids, (c) large-CP, (d) small-CP.