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ScienceDirect
Journal of Non-Crystalline Solids 354 (2008) 1598–1607
JOURNAL OF NON-CRYSTALLINE SOLIDS
www.elsevier.com/locate/jnoncrysol

Growth related properties of pentacene thin film transistors with different gate dielectrics

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Received 28 June 2007; received in revised form 19 September 2007

Abstract

We report a study on the influence of dielectric surface properties on the growth, the morphology and ordering of pentacene layers and associated consequences on the performance of organic field effect transistors (OFETs). This work mainly aims at disentangling the respective influences of surface roughness and surface energy on pentacene growth. A range of inorganic high-*k* oxides as well as polymer dielectrics were compared: Ta_2O_5 deposited by e-beam evaporation or grown by anodic oxidation, polymethylmethacrylate (PMMA) single layer or PMMA/Ta_2O_5 bi-layer. Some complementary results on anodic HfO_2 were also added. Atomic force microscopy, X-ray diffraction and infrared absorption evidenced that hydrophobicity and surface roughness drastically influence pentacene growth mechanisms. Transistors realized with the different dielectrics show characteristics well correlated to pentacene structural properties. In particularly, we point out the relationship between the grain size and the field effect mobility with the surface energy of the dielectric substrate. The general trend is that the bigger the grains, the higher the mobility but that best electrical performances of OFETs are obtained with a dielectric surface energy close to that of pentacene. This work also bears out our former results on the benefit of a polymer/high-*k* oxide bilayer dielectric configuration to improve the field effect mobility while keeping a low operating voltage.

Keyword: Thin film transistors; Polymers and organics

1. Introduction

Organic field effect transistor (OFETs) received much attention since two decades and has become the corner stone of the newly developed field called plastic electronics. Besides fantastic improvement in device performance, the mechanism of charges carrier transport in polycrystalline organic layers is still debated as evidenced by recent papers on device modeling [1]. Indeed, we are facing a double concern, say (i) the improvement of transport properties of the organic semiconductor itself and (ii) a better control of interfaces which are known to play prominent role in thin film devices. The challenge comes from the fact that the two problems are strongly interrelated. For instance, charge transport is known to take place in a conduction channel as thin as the first few monolayers of the organic semiconductor close to the interface with the gate insulator [2,3]. As a consequence, the early stage of semiconductor growth are of prime importance on the electrical properties of devices. The relationship between morphology and transport was already reported [4,5] as well as the prominent influence of grain size [6], dielectric surface properties as roughness [7–9], surface chemistry [10–13] and surface potential [14,15].

Currently, highest mobilities for OFETs based on polycristalline films have been demonstrated with pentacene films [16]. However there is, in the literature, a controversy about the relation between pentacene morphology, notably the grain size, and field effect mobility. It was already

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0022-3093/$ - see front matter © 2007 Elsevier B.V. All rights reserved.
doi:10.1016/j.jnoncrysol.2007.10.027

reported that larger grain size, and correlatively improved mobility, could be achieved by either decreasing the dielectric surface roughness or by modifying the pentacene deposition conditions and post-deposition treatments [4,17]. Moreover the use of polymeric dielectrics as polyvinylphenol (PVP) favors the formation of large grains, similarly to what obtained on smooth SiO_2, which leads to enhanced performances [18]. However, some investigations reported improved electrical transport for reduced pentacene grain size when deposited on hydrophobic surface ($\theta_{H_2O} > 90°$) as on octadecyltrichlorosilane (OTS) treated SiO_2 [4,19,20] or hydrophobic polymeric dielectric [13].

In a previous work we proposed pentacene thin film transistors (TFT) with a gate dielectric made of a polymethylmethacrylate (PMMA)/Ta_2O_5 bilayer [21,22]. Such a combination aimed at combining the respective advantages of high-k oxides and low-k polymer dielectrics to obtain stable devices operating at low voltage [23,24]. The use of high-k dielectrics alone enables a large lowering of operating voltage [25–27] but also induce polarization effect which lead to carrier self trapping and consequently to electrical instabilities and mobility degradation [22,28]. Several papers reported combination of high-k inorganic and low-k polymeric dielectric either in form of composite layer [29,30] or as polymer/high-k bilayer [21,22,31–33]. This allows to process low operating voltage device and in the mean time to get rid of polarization induced transport degradation.

This work ensues from previous published papers [21,22] and focuses on the pentacene growth, morphology and ordering on two dielectric surface, namely high-k Ta_2O_5 and low-k PMMA. Correlations between structural properties of pentacene and electrical performances of OFETs are evidenced. The influence of Ta_2O_5 deposition method was assessed by comparing reactive electron beam evaporation and anodic oxidation. Moreover thick PMMA layer only and thin PMMA layer deposited onto evaporated Ta_2O_5 were also compared.

2. Experimental

Fig. 1 gives a schematic view of the two types of bottom gate OFETs with either a single layer gate dielectric (Ta_2O_5 or PMMA) or a bilayer (PMMA/Ta_2O_5). In every case a highly doped silicon substrate was used as gate electrode. Ta_2O_5 was deposited by two different way:

- e-beam evaporation from Ta_2O_5 platelets (purchased from Cerac Inc.) in an oxygen partial pressure of 2×10^{-4} mbar: The Si substrate was kept at near room temperature during deposition. The deposition rate was 5 Å/s and the film thickness was 120 nm when only Ta_2O_5 is used or 80 nm in the bi-layer configuration. No post-deposition annealing was done.
- Anodization of a 100 nm e-beam evaporated tantalum films: the process was carried out in a tartaric acid-glycol-water solution at constant current density (0.1 mA/cm^2) up to an anodization voltage V_A in the 25–100 V range. In reported results, the oxide growth rate and the final thickness were respectively 0.11 nm/s and 34 nm [34]. No post-anodization annealing was carried out.

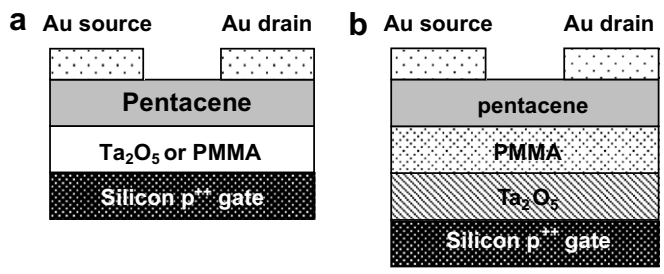

Fig. 1. Schematic structure of the OFET with (a) single layer Ta_2O_5 or PMMA a and (b) bi-layer PMMA/Ta_2O_5 gate dielectrics.

PMMA was dissolved in anisole and deposited by spin coating. The films were annealed on a hot plate at 120 °C for 5–15 min depending on the thickness of the PMMA layer in the range 40–330 nm. For devices with PMMA single gate dielectric, the thickness of PMMA was 330 nm and in the case of bi-layer gate dielectric 37 nm PMMA was deposited onto 80nm evaporated Ta_2O_5.

After deposition of the insulator a pentacene film was deposited by thermal evaporation. Pentacene deposition parameters influence the organic film morphology and consequently transistor performances [35]. For all devices, pentacene evaporation was carried out at a very low and constant rate of 0.25 ± 0.05 Å/s on the dielectric substrate maintained at 70 °C. The pentacene (purchased from Aldrich) was used as received without further purification. The devices were completed by the evaporation of interdigited Au top contact source and drain electrodes through a shadow mask. Two sets of shadow masks were used along this study. One with channel length of $L = 115$ μm and a width of $W = 1.9$ mm (mostly used for transistors with evaporated Ta_2O_5 or PMMA) and another one with $L = 100$ μm and $W = 1000$ μm usually for devices with anodic Ta_2O_5. Nevertheless, the difference is only of geometric nature and no influence of the mask dimension on device performance was observed.

Capacitance structures were also processed to determine the gate capacitance. On Ta_2O_5, Al electrodes were patterned by lithography with various capacitance areas in the range 1×10^{-4}–36×10^{-4} cm^2. In the case of PMMA, Al electrodes were evaporated through a shadow mask and the capacitance area was 5×10^{-3} cm^2. C–V measurements were carried out at RT with a HP 4284 LCR meter at 1 MHz and 1 kHz.

The transistors were characterized in air and at room temperature by using two Keithley 2400 Source-Meter units under Labview® environment.

Atomic force microscopy (AFM) images were carried out on a Smena A (NT-MDT) microscope in air, using