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Thermal behavior of floating gate oxide defects (moving bits)

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Abstract

The defect density of the oxides used in non-volatile memories (NVM) is a key parameter to the understanding of the data loss of these structures. One of the most critical phenomena responsible for this loss (in the range of oxide thicknesses used in NVM devices) is the stress induced leakage current (SILC). The origin of SILC is generally attributed to the trap assisted tunnelling (TAT); therefore, a better understanding of the evolution of the oxide defects is necessary. It is known that the leakage through the oxide defects is temperature accelerated below 100 °C. Besides, it was observed that above 100 °C, the oxide defects are annealed. To better understand the temperature behavior of the defect population, a dedicated method has been devised and applied to several baking experiments. It leads to new observations and to the correction of some biased interpretations due to unsuitable experimental methods. Indeed, in this paper, we point out the fact that the annealing effect already occurs at 60 °C. The activation energy was calculated and found independent from both the electrical field across the oxide and the number of program/erase (P/E) cycles. The temperature behavior of the leakage is found to be more complex than what was reported in the literature: it is a balance between two opposite phenomena. Based on that, a new model describing the defect population evolution is proposed.

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Keywords: Oxide defects; Defect annealing; High temperature; SILC; Moving bits

1. Introduction

The floating gate (FG) concept has been extensively studied and used for non-volatile memory (NVM) devices. The FG based memory stores digital information by means of charge storage in the floating polysilicon gate. As a matter of fact, the NVMs are unstable devices; indeed, once the FG of the device is charged (or discharged), it is put into a state of electrical non-equilibrium. The natural trend to come back to the equilibrium leads to the charge leakage through the oxide surrounding the FG. This effect limits the data retention (DR) of such structures. Therefore, the DR depends on the quality of the dielectrics isolating the FG.

Silicon dioxide (SiO_2) is generally used as dielectric. It has defects due to the fabrication process and applied electrical stresses when moving electrons to or out of the FG (respectively, programming or erasing the memory). These defects are known to facilitate charge leakage by means of a physical phenomenon referred to as stress induced leakage current [1].

SILC degrades the DR by discharging the FG of a very few bits in a memory array. Those '*moving bits*' define the DR capability of the full array as their electrical characteristics drift quickly. Therefore, it is necessary to understand the behavior of the SiO_2 defects.

In this paper, the thermal behavior of the defect population is studied. The elevated temperature is known to increase the FG charge leakage; however, a few papers in the literature have pointed out the annealing effect of the temperature that decreases the defect population.

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This population behavior (depending on the temperature) is still not completely understood. This study aims to make new observations in order to model the defect population evolution.

2. Experimental details

2.1. Material

The FG structure used in this study is the HIMOS™ cell [2,3] (see Fig. 1). The insulator layer concerned by the defects inducing the leakage is the tunnel oxide. This oxide is processed using a diluted oxygen wet oxidation recipe. Its thickness is in the range known to be temperature dependent (around 80 Å) [4,5].

Memory devices of 1.4 Mega bits are used to point out the defects behavior. All the bits of a device are programmed/erased then are kept in an oven at a given temperature: this will be referred to as a REtention Test (RET). The devices are periodically read out (at room temperature) to scan the drift of their threshold voltage which depends on the charge stored in their FGs.

2.2. Methodology

The moving bits are those bits whose threshold voltage moves faster than that of intrinsic bits. As a consequence, they move out of the main distribution and form a tail which becomes larger and larger in time (Fig. 2). Two devices having the same conditions of retention (temperature, retention duration, amount of cycles...) must have similar distribution tails whatever their initial threshold voltage. This is because the leakage current that makes the bit move decays drastically when the threshold voltage gets closer to its equilibrium value [2]. This important characteristic enables us to describe the moving bit performance of a device by plotting the number of bits failing at a given failure criterion (Fig. 2). We define a failing bit as the moving bit whose threshold voltage crossed a fixed value used as a failure criterion. The bit failure rate (BFR) is the ratio between the number of failing bits and the number of bits in the array. It provides information about the leakage of the FG charges.

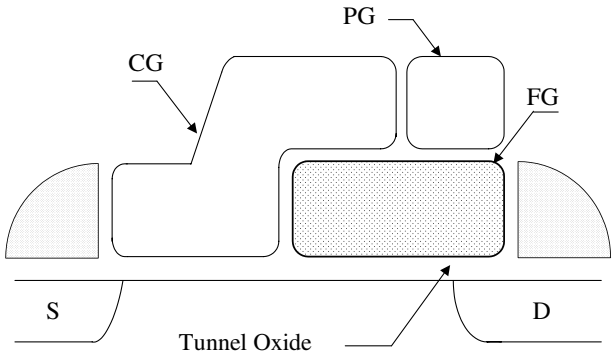

Fig. 1. Cross section of the HIMOS™ cell.

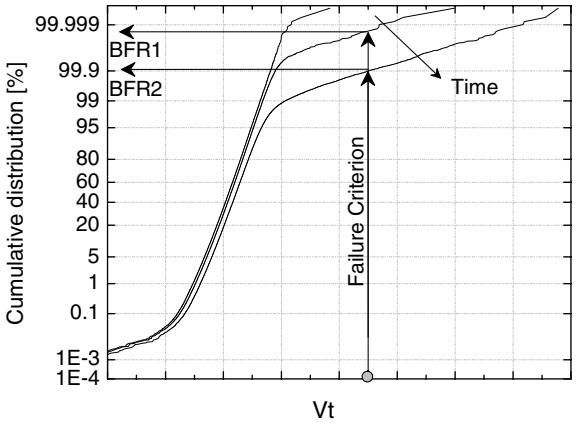

Fig. 2. Example of a cumulative distribution showing the evolution of the V_{ts} of a memory array with time. The BFRs are extracted at the intersection of the tails with the failure criterion.

3. Results

For result consistency, all experiments shown in this paper used at least two devices per condition. Moreover, most of the experiments have been repeated at least once.

3.1. Confirmation of published observations

It is commonly accepted that DR depends on temperature. More specifically, it is shown that in case of oxides thicker than 8 nm the moving bits are temperature dependent [4,5].

The first observation is a curing effect of high temperature bakes (150–250 °C according to Refs. [4,5]). This was confirmed at 150 °C with pre-bake performed at packaged device level (and at 270 °C with pre-bake done at wafer level).

The second observation is the existence of the worst case temperature around 60 °C and 85 °C. The characterizations of our material (Fig. 3) clearly show this worst case around 60 °C while 85 °C is slightly worse than room temperature (RT).

The commonly accepted explanation is the following: at low temperature, the leakage mechanism is thermally activated with activation energy between 0.26 eV and 0.81 eV depending on the number of P/E cycles [5]. Above 100 °C, the defects that make some bits move are annealed out so that 'no' moving bit is seen.

3.2. New observations

As already mentioned, the worst case reported in the literature is 60–85 °C. We reproduced the experiment and confirmed this observation after 24 days (~600 h) of RET (Fig. 3); however, the test showed different worst cases at medium and long term experiment (see Fig. 4). Indeed, at the early stage of the RET (1 week; 168 h), the worst case temperature seems to be 85 °C followed by the 60 °C and then by RT. Then, from 1 week to 4 weeks