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CHE and CHISEL characterization procedure for compact Flash cell model

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Abstract

The objective of this paper is to present a CHE (Channel Hot Electron) and CHISEL (CHannel Initiated Secondary ELectron) characterization procedure for a compact Flash memory cell model. As a core element of the Flash memory model, a Philips MOS Model (MM11) model has been used coupled with the charge neutrality expression in the structure. This pragmatic model takes into account the different injection mechanism (CHE, CHISEL and Fowler–Nordheim). The characterization procedure developed under ICCAP to extract the full model card including the CHE and CHISEL current parameters are detailed. This model has been successfully implemented in ELDO.

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1. Introduction

Flash have become over the last few years a very relevant choice for any application requiring non volatile semiconductor memory and represent 50% of the NVM market [1]. This trend is strongly influenced by the market of portable devices such as smart card or mobile communication media. To follow the permanent evolution of these applications, Flash memory design constraints in term of integration and performances have to be continuously enhanced. Therefore, circuit simulations including Flash memory become a corner stone for the design of these kinds of application. From these preliminary remarks, it becomes essential to introduce compact and accurate simulation model of the Flash memory cell. One of the main aspect of Flash modeling for design purpose concerns the simulation of gate tunneling current coupled with a designer well known transistor model such as MM11 [2]. The memorization mechanism of the Flash is achieved by controlling the threshold voltage of the cell which depends on the amount of charges trapped in the floating gate. The threshold voltage of a cell can be shifted to a high state (program mode) or low state (erase mode) corresponding respectively to electrons injection into the floating gate or electrons release. The program mode involves Channel Hot Electron (CHE) and CHannel Initiated Secondary ELectron (CHISEL) injection mechanisms [3–6], whereas the erase mode involves Fowler–Nordheim (FN) tunneling mechanism [7]. In this paper, a model of a floating-gate Flash cell is presented based on the MM11 model [2] coupled with the charge neutrality approach [8]. This pragmatic model takes into account the geometric dependencies of the cell. Moreover, the characterization procedure developed under ICCAP, a experimental data collection software, to extract the MM11 model card as well as the tunneling current parameters is presented with emphasis on the CHE and

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CHISEL extraction procedure. This model has been successfully implemented in the electrical simulator ELDO [9].

The paper is organized as follows. Section 2 describes the Flash cell model with emphasis on the static and dynamic behaviors of the NOR-type Flash memories. This section describes in detail how the tunneling currents are plugged on the MM11 model coupled with the charge neutrality formulation. In Section 3, the characterization procedure developed to extract all the model parameters using ICCAP is presented with emphasis on the CHE and CHISEL extraction. Finally, Section 4 gives some concluding remarks.

2. Flash cell model based on a MM11 transistor formulation

The Flash cell is a stacked gate transistor or Floating Gate Transistor (FGT); the Fig. 1 illustrates the geometry of a ST-Microelectronics cell thanks to a TEM cross-section, where T_{ono} is the inter-polysilicon oxide–nitride–oxide thickness, T_{ox} is the oxide thickness over the channel, W_{pp} is the floating gate width, L_{pp} is the floating gate length and W, L the width and length of the channel, respectively. The approach used to develop a Flash FGT model is based on the use of the charge neutrality approach coupled with the MM11 formulation. In this approach, the charge neutrality, including the charge stored in the floating-gate, is applied to determine the floating gate potential from which all the variables can be calculated in the MM11 model formulation. Knowing all the variables of the MM11 formulation, the current equations used to model injection currents can be solved. Consequently, the description of the Flash model, represented Fig. 2, includes:

- A MM11 description to simulate the intrinsic transistor that appears between the floating gate (FG), the source node (S), the drain node (D) and the bulk (B).
- An extra capacitor C_{pp} between the control gate (CG) and the floating gate (FG).
- Extra current sources for CHE, CHISEL and FN.

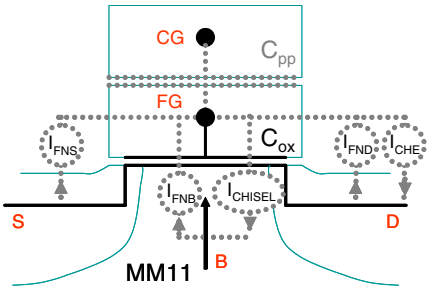

Fig. 2. Flash cell model description overview with programming current sources for CHE, CHEI and Fowler–Nordheim mechanism in source, drain and substrate region (respectively I_{FNS}, I_{FND} and I_{FNB}).

2.1. Static model

The Gauss law applied to the surface including the floating gate allows us determining the charge Q_{FG} trapped in the floating gate

$$Q_G + C_{pp} \cdot (V_{FG} - V_{CG}) + C_{GD} \cdot (V_{FG} - V_D) + C_{GS} \cdot (V_{FG} - V_S) - Q_{FG0} = 0, \quad (1)$$

where C_{pp} is the interpoly capacitance, V_{FG} the potential of the floating gate, C_{GD} and C_{GS} are respectively the drain and source overlap capacitance, V_{CG} the voltage applied on the control gate, V_D the voltage applied to the drain and V_S the voltage applied to the source. The charge Q_{FG0} represents, when necessary, the initial charge trapped in the floating gate. The charge Q_G is the gate charge calculated by using the charge model part of the MM11. This charge is a function of the depletion charge and of the inversion charge. These two charges are calculated knowing a set of variables and more specifically V_{FG}, the potential of the floating gate. Consequently, the Eq. (1) is an implicit equation of V_{FG}. By solving this equation V_{FG} is calculated for all possible potential applied on the Flash cell. Knowing the potential V_{FG}, applied on the gate of the MM11 instance, all the variables of the model can be

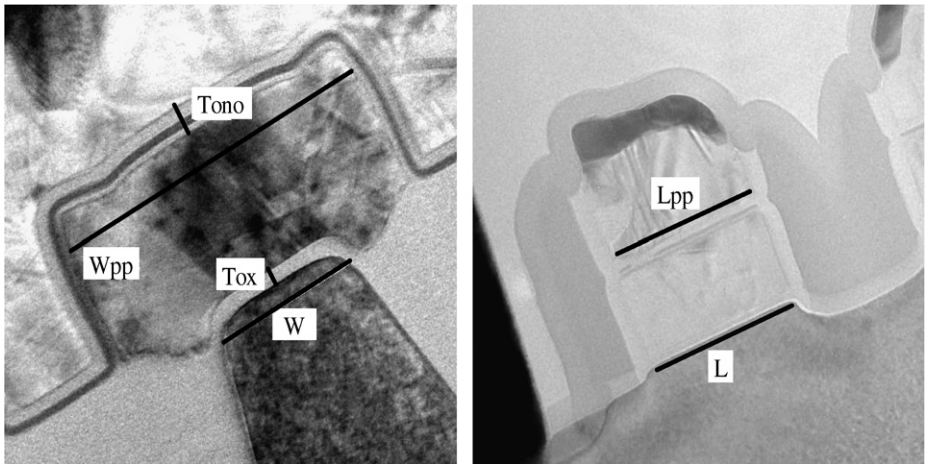

Fig. 1. Cross sections of a Flash cell with main geometrical parameters representation.