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Impact of high-permittivity dielectrics on speed performances and power consumption in double-gate-based CMOS circuits

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Abstract

The performances of double-gate (DG)-based CMOS circuits with high-κ dielectrics are analyzed in terms of inverter delay and static power consumption. We show that the use of a high-κ layer as gate dielectric degrades the short-channel immunity of DG devices and increases the power consumption, but for a gate dielectric relative permittivity κ lower than 50, the circuit performances still fill the ITRS requirements. Moreover, the use of a double gate dielectric layer (thin SiO_2 oxide and high-κ layer) not only does not degrade the circuit performances, but even ameliorates the inverter speed. Finally, the analysis of back gate misalignment in DG circuits with double gate dielectric layer illustrates that the variation of the inverter performances induced by the back gate misalignment in these high-κ-based devices is comparable with that of the conventional (SiO_2 oxide layer) structure.

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1. Introduction

Double-gate (DG) metal–oxide–semiconductor field-effect transistor (MOSFET) and related multiple-gate device architectures are nowadays widely identified as one of the most promising solutions for nanoscale integration [1,2]. These devices present an excellent I_{on}/I_{off} trade off, very good control of short-channel effects and potentially higher channel conductivity. In order to prevent direct gate tunnelling in very thin oxides envisaged for the end-of-the-roadmap nodes, the SiO_2 is replaced by alternative materials with higher permittivity and greater physical thickness [3]. However, the introduction of these high-κ dielectrics poses several problems, such as bi-dimensional electrostatic effects which may have a dramatic impact on the device performances when the gate dielectric thickness becomes comparable to the device gate length [4–7]. In this work, we analyze via numerical simulation the impact of the use of high-κ gate dielectrics or of double-layer gate dielectric on the performances of DG-based CMOS (Complementary MOSFET) inverters. In a second step, we study the impact of the back gate misalignment on the operation of the CMOS inverter composed of DG MOSFETs with high-κ gate dielectrics. Since the fabrication of planar DG MOSFET with self-aligned gates is a difficult technological task, the back gate could not be perfectly aligned with respect to the top gate. Several configurations can occur: (1) the back gate is shifted towards the source or drain region with respect to the top gate, (2) the back gate is larger than the top gate (and overlaps the source and drain regions), (3) the back gate is over-etched and then the gate underlaps the channel. All these configurations introduce parasitic elements (such as additional series resistances and capacitances), which affect the operation of the devices and associated circuits. Configurations where the two gates are not perfectly aligned have been already studied in the literature for conventional DG devices with SiO_2

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gate dielectrics [8–10]. In this paper, we investigate the impact of the back gate misalignment/overlap/underlap on the delay and power consumption of CMOS inverters composed from DG MOSFETs having high-κ dielectric gate stack.

2. Simulations details

The DG architecture simulated in this work is shown in Fig. 1(a). The structure is symmetric, with intrinsic thin silicon film ($t_{Si} = 5$ nm), highly doped source and drain ($N_{SD} = 3 \times 10^{20}$ cm^{-3}), a midgap metal gate and lateral SiO_2 spacers covering the source and drain regions. Two gate stack configurations are considered: (1) single-layer gate dielectric (high-κ with different κ values from $\kappa = 10$ to $\kappa = 100$) and (2) double-layer gate stack composed from an interfacial oxide layer (SiO_2) and a high-κ layer. All these structures have been calibrated to fill the ITRS 2005 roadmap [11] requirements for the 2011 node with $L = 16$ nm physical gate length. These different gate stack configurations have been designed with the same EOT (equivalent oxide thickness) = 8 Å, as reported in Table 1. The permittivity values considered here correspond to real materials such as HfO_2 ($\kappa = 20$), TiO_2 ($\kappa = 80$–110) and La_2O_3 ($\kappa = 20$) [12]. Fig. 1(b) presents the schematics of a CMOS inverter composed of DG MOSFET with n-channel (NMOSFET) and p-channel (PMOSFET) as simulated in this work. The DG structures considered for the analysis of the back gate misalignment are shown in Fig. 2(a)–(e). Firstly, we consider the case where the back gate has the same length than the top gate, but is shifted towards the source side (DG-S-mis, Fig. 2(b)) or the drain side (DG-D-mis, Fig. 2(c)). We also studied here two other usual cases when the back gate is not aligned to the front gate: the case of a back gate longer than L_G and which overlaps the front gate on both source and drain sides (DG-overlap, Fig. 2(e)) and the case of a back gate smaller than the front gate, inducing a back gate underlap of the channel on both source and drain sides (DG-underlap, Fig. 2(d)). The back gate misalignment length, l_{mis} (defined in Fig. 2) is considered zero for the reference structure (Fig. 2(a)), positive for DG-D-mis and DG-overlap structure and negative for DG-S-mis and DG-underlap configuration. 2D numerical simulations of the DG MOSFET have been performed using the Drift–Diffusion transport model implemented in Atlas (Silvaco) tool [13]. At the best of our knowledge, this is the first study performed using the Atlas tool on such high-κ-based DG structures. The main parameters (mobility, carrier statistics and recombination) were expressed by a set of models universally used for the CMOS technology [13]. Simulation at the circuit level has been performed using the Mixed-Mode module [13], which allows simulating the static and transient behavior of small circuits. Since compact models for DG MOSFET are not implemented in Mixed-Mode, both the NMOSFET and the PMOSFET which compose the CMOS inverter have been numerically simulated.

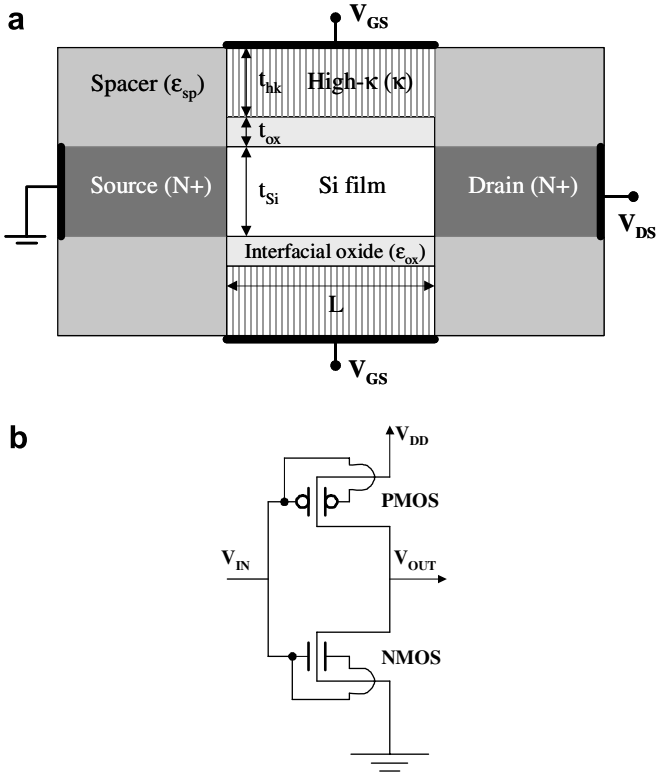

Fig. 1. (a) Schematics of DG MOSFET and associated geometrical parameters used in this work; (b) schematics of a CMOS inverter based on DG MOSFETs.

Table 1
Geometrical parameters of the dielectric stack for the DG structures considered in this work

Single-layer gate dielectrics ($t_{ox} = 0$)		Double-layer gate dielectrics ($t_{ox} = 5$ Å)		Double-layer gate dielectrics ($t_{ox} = 6$ Å)		κ	EOT (Å)
Name	t_{hk} (Å)	Name	t_{hk} (Å)	Name	t_{hk} (Å)		
REF	0.0	–	–	–	–	–	8.0
K10	20.5	–	7.69	–	5.13	10	8.0
K20	40.1	–	15.38	–	10.25	20	8.0
K30	61.5	–	23.08	–	15.38	30	8.0
K50	102.6	–	38.46	–	25.64	50	8.0
K70	143.6	–	53.85	–	35.90	70	8.0
K100	205.2	A	76.9	B	57.3	100	8.0