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High speed anisotropic etching of Pyrex® for microsystems applications

Abhijat Goyal, Vincent Hood, Srinivas Tadigadapa *

Department of Electrical Engineering, Pennsylvania State University, 111J EE West Building, University Park, PA 16802, USA

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Abstract

We report high speed etching of glass (Pyrex® 7740) substrates using an inductively coupled plasma (ICP) reactive ion etching (RIE) process employing sulfur hexafluoride/argon (SF_6/Ar) based chemistry. Electroplated Ni over a patterned Cr/Au seed layer was used as the hard mask for etching. Detailed process characterization was performed by varying the process parameters which include substrate temperature, ICP power, substrate power, operating pressure, distance of substrate holder from ICP source and composition and flow rates of the etching gases. An rms surface roughness of 1.97 nm at a high etch rate of 0.536 μm/min was achieved by process optimization. We used least square fit to find the direction of maximum variance in the process parametric space and to reduce the dimensionality of the process parametric space. The etch rate was then linearly related to a new variable termed as the etch rate number.

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1. Introduction

To date, efforts in silicon dioxide (glass) etching, have been primarily directed towards realizing features for microelectronics applications such as interconnect vias [1], waveguides [2], phase shift masks [3], etc. Hence, process optimization has traditionally aimed at increasing the selectivity of silicon dioxide over silicon substrate [4], reducing gate oxide damage [5], decreasing sidewall roughness [6], and increasing sidewall angle of the etched feature [7]. With the advent of microelectromechanical systems (MEMS) and microsystems in the last decade, focus has shifted to high aspect ratio etching of silicon dioxide for applications in microfluidics [8], microsensors [9], and laboratory on a chip applications. Many of these applications require greater than 100 μm of silicon dioxide (glass) etching while maintaining the surface finish, with rms surface roughness of less than 5 nm [10,11]. Hence, these applications impose additional new requirements on glass (Pyrex® 7740) etching processes such as high etch rate, high selectivity to masking material, high anisotropy, low surface roughness for mirror polish, uniformity of etch across the wafer and within a pattern [12], etc.

Traditional reactive ion etching (RIE) processes are limited by the fact that the substrate power and RF plasma power are coupled to each other often resulting in etch non-uniformity across the wafer, low density of plasmas, and limited control over the processing conditions. However, in an inductively coupled plasma (ICP) RIE system, the substrate power and the coil power are independent of each other thus providing excellent control over plasma density (controlled by ICP power) and energy of etchant ions (controlled by substrate power) [13]. As a result, plasma can be generated even at relatively low pressures in the range of 10^{-3}–10^{-4} Torr. At such low pressures, the plasma in traditional RIE systems is not stable. Low processing pressure is necessary for rapid removal of etching products from the surface and also for the removal of stray particles generated from the masking material,

* Corresponding author. Tel.: +1 814 865 2730; fax: +1 814 865 7065.
E-mail address: sat10@psu.edu (S. Tadigadapa).

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substrate holder and walls of the reaction chamber. The presence of stray particles results in micro-masking wherein the micro-particles or reaction products on the substrate shield the surface from the etchant species resulting in surface roughness, micro-trenching and formation of plateau-like structures. Additionally, the increased mean free path at low pressures improves the anisotropy of the etch by minimizing the randomizing collisions between the radicals, ions and other plasma species. In this paper, we present a detailed study of the various process parameters (ICP power, substrate power, operating process pressure, gas flow rates, ratio of gas flows, substrate temperature and distance from source) on the etch rate of features in Pyrex® 7740 glass substrates. Pyrex® 7740 is known to have a typical composition of SiO_2 (79.6%), B_2O_3 (12.5%), Na_2O (3.72%), Al_2O_3 (2.4%) and K_2O (0.02%). Fig. 1 shows a schematic drawing of the Alcatel AMS 100 ICP-RIE etcher used in this work.

2. Experimental details

The 4″ Pyrex® 7740 wafers (double sided polished) were cleaned thoroughly with acetone/isopropyl alcohol (IPA) followed by piranha clean (1:1 H_2SO_4:H_2O_2) for 1 h. A seed layer, consisting of 200 nm of gold with 20 nm of chromium as an adhesion layer, was subsequently e-beam evaporated on the cleaned glass (Pyrex® 7740) surface. The etch patterns were then delineated on the seed layer using standard lithography and wet etching steps [14]. The patterned 4″ wafers were diced into individual 1″ dies. A thick layer (5–10 μm) of Nickel was then electroplated onto the seed layer on the 1″ dies. The fabrication sequence is illustrated schematically in Fig. 2. Control over the quality of the electroplated nickel was maintained using constant stirring of the electroplating solution and the use of a pulsed power supply. This was necessary to minimize the formation of stray particles acting as micro-masks. The electroplated dies were then clamped into a substrate holder made of aluminum. The temperature of the substrate holder was controlled using a chiller and back side cooling of the aluminum holder using helium gas as shown in Fig. 1. A standard run time of 1 h was used for all the samples. SF_6/Ar based chemistry was used for the etching of the samples. The etch rate was determined from the step height of the etched feature which was measured using a stylus profilometer.

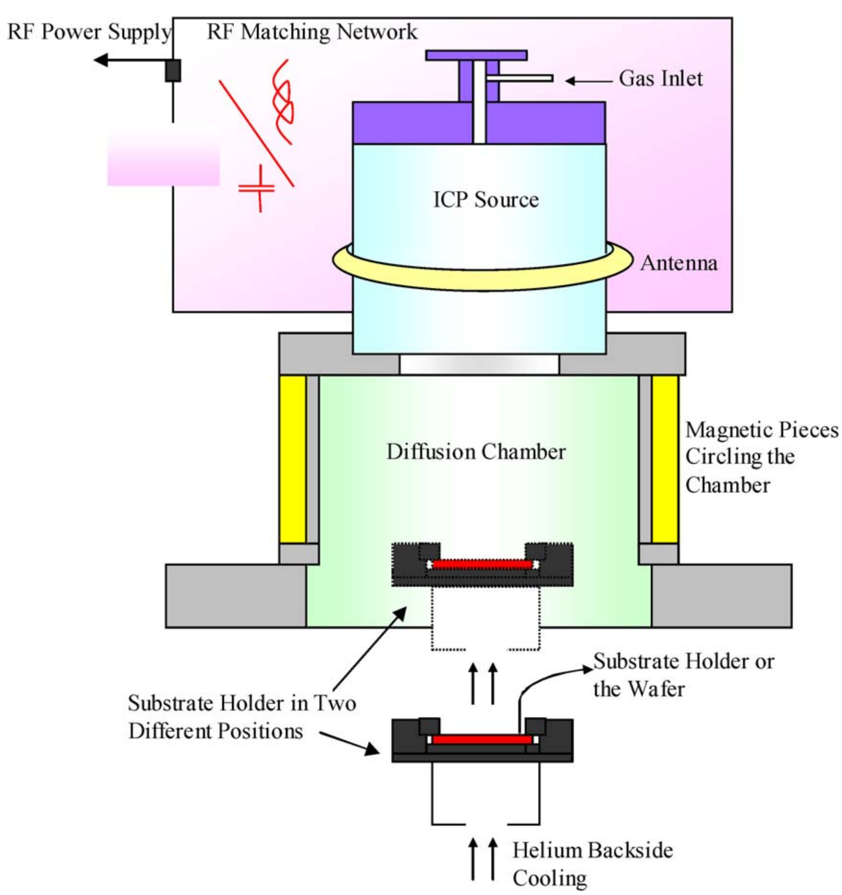

Fig. 1. Schematic illustrating the ICP RIE set up used in this work. The vertical position of the substrate holder which is backside cooled using He can be adjusted with respect to the ICP source. Also, the diffusion chamber is lined with magnets to increase the density of the plasma.