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Improvement of the short channel effect in PMOSFETs using cold implantation

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ABSTRACT

In this paper, to suppress transient enhanced dopant diffusion and improve short channel effects, cold implantation (cold-IIP) was applied to contact PLUG implantation in P-channel metal oxide semiconductor field effect transistors (PMOSFETs). A shallow dopant profile was formed by the suppression of transient enhanced diffusion (TED) due to the reduction of end-of-range (EOR) defects. Threshold voltage roll-off and off current (I_{off}) increment, which are caused by a reduction in the distance between the gate and contact, were improved compared with room temperature implantation (RT-IIP). Additionally, the drain induced barrier lowering was improved, and the on-current improvement was attributed to reducing the contact resistance through the reduction of EOR defects. The contact resistance was reduced by ~6% of the RT-IIP. In the DRAM device, the standby current at a short propagation delay time (t_{PD}) was reduced effectively due to the decrease in the I_{off} and contact resistance for the cold-IIP case.

1. Introduction

Short channel effects (SCE) such as the reduction of the threshold voltage (V_{TH} roll-off), degradation of the sub-threshold slope, and velocity saturation are limiting factors for device integration as devices are scaled down [1]. For improvements in the SCE, junction technology that reduces the junction depth has been studied and adopted to metal oxide semiconductor field effect transistor (MOSFET) fabrication. When producing a shallow junction, weak lateral spreading is desirable for control of SCE, while the source and drain resistances have to be as low as possible [2]. Cold implantation (cold-IIP) [3], germanium (Ge) pre-amorphization implantation (PAI) & carbon (C) co-implantation [4], and heavy dopant (indium to NMOS) implantation [5,6] were proposed for fabrication of the shallow junction. Ge PAI & C co-implantation technology was used to suppress transient enhanced diffusion (TED) and to contain the diffusion of boron (B) or phosphorus (P) used to dope N/PMOS [4,7]. However, Ge PAI & C co-implantation causes the increment in the sheet resistance and junction leakage current because of additional Ge dopants and induced damage [8,9], and indium implantation increases the sheet resistance due to acceptor freeze-out effect [10]. Cold-IIP focuses on engineering damages caused during implantation and is used to increase the amorphous layer in place of Ge PAI [11,12]. In this paper, the effects of cold-IIP in terms of the amorphous layer thickness, dopant diffusion and device performance (V_{TH}, junction leakage current, and contact resistance) were investigated through transmission electron microscopy (TEM), secondary ion mass spectroscopy (SIMS) and electrical analyses.

2. Experiments

For the fabrication of a PMOSFET, arsenic (As) halo implantation was performed after the gate was etched and a lightly doped drain (LDD) region was formed. A sidewall spacer was then formed and S/D P^+ (B) implantation was performed. B contact PLUG implantation was performed with the largest dose to form an ohmic contact. For the first part of the experiment, TEM analysis was conducted to

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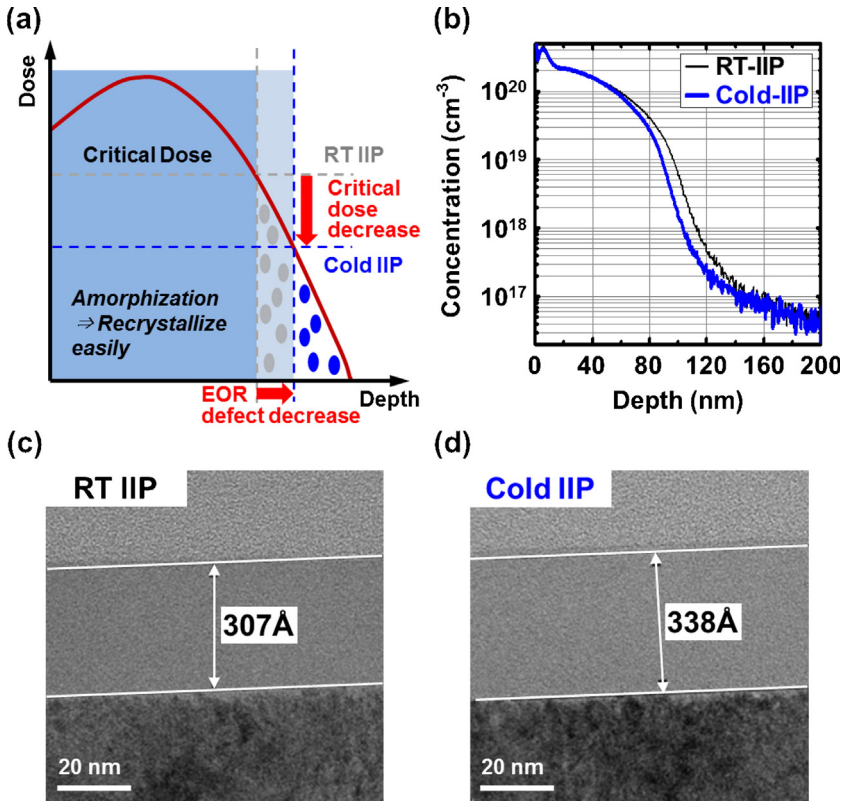

Fig. 1. (a) Schematic of the cold-IIP mechanism. When the cold-IIP technique is applied on Si, the amount of critical dose is decreased, thereby reducing the EOR defect area. (b) SIMS profile comparison between RT-IIP and cold-IIP. (c), (d) TEM images of RT-IIP and cold-IIP.

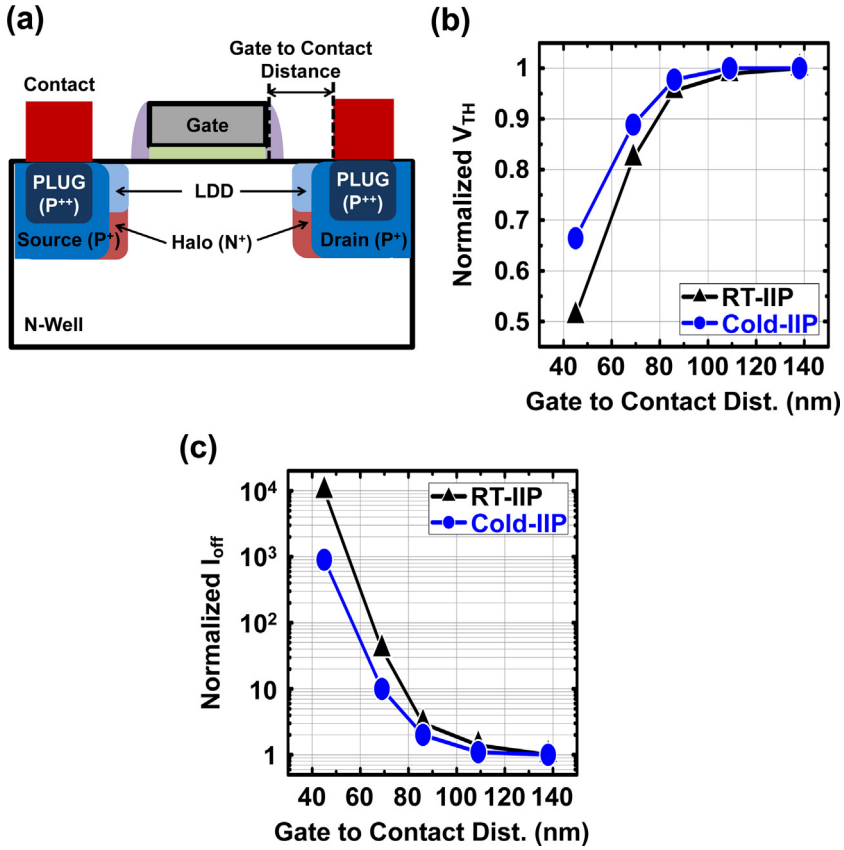

Fig. 2. (a) Schematic of the PMOS structure. (b) V_{TH} reduction according to reduction of the distance between the gate and the contact. (c) I_{off} increment according to shortening of the distance between the gate and the contact ((b) and (c) normalized with 140 nm).