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Bias-induced instability in an intrinsic hydrogenated amorphous silicon layer for thin-film solar cells

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ABSTRACT

In this article we present a mechanism for creating metastable defects in intrinsic hydrogenated amorphous silicon (a-Si:H) layers by changing the flow-rate ratio of SiH_4 and H_2. This is an important cardinal property that restricts the performance of both solar cells and thin-film transistors (TFT). Light or electrical bias results in generation of metastable dangling bonds. We evaluated the gas flow-rate ratio dependence of current decrease before and after application of electrical bias stress. Furthermore, we produced an a-Si:H TFT for comparison with a single-layer a-Si:H. Intrinsic layers deposited by SiH_4 to H_2 flow-rate ratios of 1:3 exhibited greater resistance to stress. In a-Si:H single layer experiment, we got a similar result, samples with SiH_4 and H_2 flow-rate ratios of 1:3 exhibited less decrease in current after application of electrical bias stress. These results will facilitate fabrication of more-stable a- Si:H thin film p-i-n solar cells.

1. Introduction

Hydrogenated amorphous silicon (s-Si:H) is widely used in thin-film transistors (TFTs) and solar cells. Metastable defects cause degradation of amorphous silicon thin-film applications. Metastable dangling bond defects are formed in an a-Si:H, whenever it is illuminated [1], and charge carriers accumulate [2] or temperature increases [3]. Creation of defects by illumination, known as the Staebler-Wronski effect [1], is a major cause of efficiency limitation in amorphous silicon solar cells. Metastable defects in a-Si:H solar cells can also be generated when the cells are subjected to prolonged forward bias without illumination [4]. With regard to TFTs, electrons are injected into the channel region and break weak Si-Si bonds increasing the density of the dangling bonds in a-Si:H layers, which leads to a threshold voltage shift [5,6].

The instability of a-Si:H layers prevents their use in devices. The generation of metastable defects by illumination [7,8] and temperature changes [9,10] has been investigated extensively. The generation of metastable defects by electrical bias is, however, insufficiently understood. In this paper, we investigate defect creation by electrical bias in intrinsic a-Si:H layers deposited using SiH_4 and H_2 gases with flow-rate ratios of 1:0, 1:1, 1:3 and 1:5.

2. Experimental

a-Si:H films were deposited on Eagle 2000 glasses by VHF (60 MHz) PECVD. The H_2/SiH_4 gas flow-rate ratio was varied from 0 to 5, and the other deposition conditions were kept constant—power at 30 W, temperature at 200 °C and working pressure at 200 mTorr. The film thickness was 200 nm. The a-Si:H films were prepared as finger joint shape of photoconductor as seen in Fig. 1. The a-Si:H photoconductors were annealed at 180 °C for 1 h to ensure identical initial conditions. We measured the spectral response of a-Si:H photoconductors before and after 15 V bias stress at room temperature up to 3600 s.

A series of amorphous silicon TFTs with an inverted-staggered structure was prepared. An amorphous silicon film was deposited to a thickness of 100 nm with various $H_2:SiH_4$ gas ratios. The gate insulator was 200 nm thick silicon nitride (SiN_x). We measured the bias dependence of the threshold voltage shift as follows. First, the samples were annealed to 180 °C for 1 h to ensure identical initial conditions and to ensure negligible charge injection into the SiNx. Electrical properties were measured using a programmable

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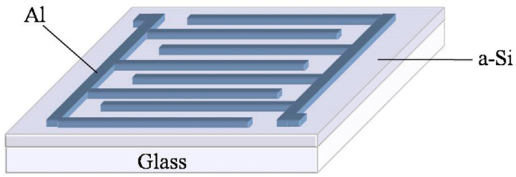

Fig. 1. Schematic of a finger-joint-shape photoconductor.

Table 1
Deposition conditions of intrinsic amorphous silicon layers.

Gas Flow			Temp (°C)	Power (W)	Depo. Time	Pressure (mTorr)
SiH4 (sccm)	H2 (sccm)	Ratio				
30	0	1:0	200	30	4 m 30s	200
30	30	1:1			5 m	
30	90	1:3			6 m 30s	
30	150	1:5			8 m 20s	

Keithley 617 electrometer. Bias stress of 15 V was applied to gate (V_G) of the transistor for 3600 s at room temperature (Table 1).

3. Results and discussion

Typical threshold voltage shifts (ΔV_T) are shown in Fig. 2. The ΔV_T differed according to the SiH_4:H_2 gas ratio.

The ΔV_T in a-Si:H TFTs are due to the charge trapping in SiN_x, mainly through tunneling and the creation of metastable defects in the a-Si:H channel layer near the gate insulator [11–13]. Charge trapping in the gate insulator becomes larger at higher gate biases, while metastable defects are generated at gate biases of 15–20 V [14,15]. Generation of defects in a-Si:H TFTs due to prolonged bias has been reported to be similar to that induced by illumination [7]. In our experiments, ΔV_T differed according to film deposition gas flow rate. The a-Si:H TFT deposited with gas flow-rate ratio of SiH_4 and H_2 of 1:3 exhibited the smallest shift in threshold voltage of 4.45 V (Fig. 2(c)). Since the gate bias of 15 V was applied to each transistor equally, the change in ΔV_T directly denotes the amount of thin film defects generated. In other words, the a-Si:H layer deposited by a SiH_4: H_2 ratio of 1:3 has considerable bias stress durability. In contrast, the a-Si:H TFT deposited by gas flow-rate ratio of SiH_4 and H_2 of 1: 0 exhibited a 5.27 V shift in threshold voltage (Fig. 2(a)) which was the largest. This result indicates that hydrogen likely plays a role in stabilizing the defects, as is generally considered.

Fig. 3 shows ΔV_T versus bias stress time for TFTs at room temperature. During the entire stress time, a-Si:H TFT with gas ratio of 1:3 showed a small ΔV_T value. In contrast, the a-Si:H TFT with gas ratio of 1:0 exhibited a large ΔV_T value during the whole stress time.

The a-Si:H photoconductors produced using four different gas ratio deposition conditions were subjected to 15 V bias stress for 1 h (3,600 s) at room temperature. The spectral response of the a-Si:H photoconductors was measured (Fig. 4). By comparing the photo-currents, we determined which layer shows the least degradation in the presence of bias stress.

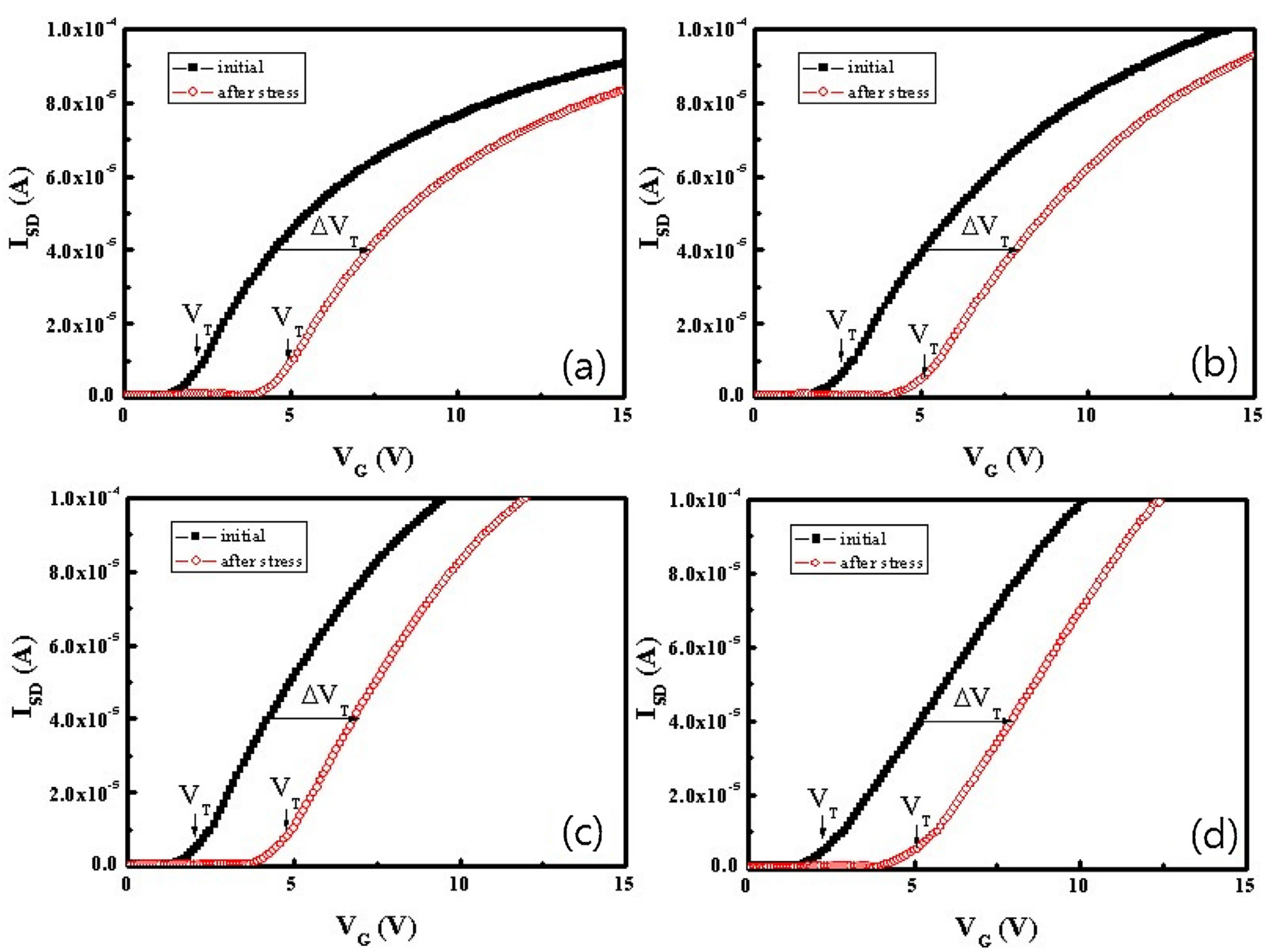

Fig. 2. Threshold voltage shifts due to 15 V gate bias as a function of SiH_4: H_2 gas ratio. (a) SiH_4: H_2 = 1: 0, (b) SiH_4: H_2 = 1: 1, (c) SiH_4: H_2 = 1: 3, and (d) SiH_4: H_2 = 1: 5.