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Time-dependent of characteristics of Cu/CuS/n-GaAs/In structure produced by SILAR method

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ABSTRACT

The aim of this study is to explain effects of the ageing on the electrical properties of Cu/*n*-GaAs Shottky barrier diode with Copper Sulphide (CuS) interfacial layer. CuS thin films are deposited on n-type GaAs substrate by Successive Ionic Layer Adsorption and Reaction (SILAR) method at room temperature. The structural and the morphological properties of the films have been carried out by Scanning Electron Microscopy (SEM) and X-Ray Diffraction (XRD) techniques. The XRD analysis of as-grown films showed the single-phase covellite, with hexagonal crystal structure built around two preferred orientations corresponding to (102) and (108) atomic planes. The ageing effects on the electrical properties of Cu/CuS/n-GaAs/In structure have been investigated. The current–voltage (*I–V*) measurements at room temperature have been carried out to study the change in electrical characteristics of the devices as a function of ageing time. The main electrical parameters, such as ideality factor (n), barrier height (Φ_b), series resistance (R_s), leakage current (I_0), and interface states (N_{ss}) for this structure have been calculated. The results show that the main electrical parameters of device remained virtually unchanged.
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1. Introduction

Metal-semiconductor (MS) junctions are generally fabricated by evaporation of the metal on the semiconductor surface. These junctions play an important role as electrical contacts for semiconductor samples and devices. The interface properties of MS rectifying contacts have a dominant influence on the device performance, reliability, and stability. Unstable contacts result barrier height changes, increased leakage current, and other undesirable effects that degrade the electrical performance of the device. The current transport across a MS junction is of interest to material and device physicists. MS junction is widely studied and many attempts have been made to understand their behavior [1–5]. It has been generally assumed that the thin interfacial layer between the metal and semiconductor is uniform and has distinct effect on the behavior of MS junctions [6–10]. Control of the barrier height is critical to the successful operation of devices based on MS contacts. Thus it is desirable that the MS interface barrier heights to be kept in various ranges according to the application purposes [11]. However, despite years of extensive research and widespread use of Schottky contacts in device technology, the fundamental mechanism responsible for the formation of the Schottky barrier is still not fully understood [12].

One of the most interesting properties of any MS interface is its Schottky barrier height. The Schottky barrier height is the rectifying barrier for electrical conduction across the MS junction and, therefore, is of vital importance to the successful operation of any semiconductor device. The magnitude of the Schottky barrier height reflects the mismatch in the energy position of the majority carrier band edge of the semiconductor and the metal Fermi level across the MS interface. The Schottky-Mott theory proposes that the Schottky barrier height depends sensitively on the work function of the metal. However, this prediction has received little support from experiment. The Schottky barrier height measured in actual experiments often showed some dependence on the preparation of the MS interface, which indicates that the Schottky barrier height depends more than just the work function of the metal. When a metal and semiconductor are brought into contact, the atomic position and the charge distribution of the surfaces will change. Both the metal work function and semiconductor work function has volume and surface contributions. The volume contribution arises because of the crystal lattice's periodic potential, whereas the surface contribution is attributable to any surface dipoles. When the periodic structure of a crystal lattice is terminated at a surface, electronic states particular to the surface are created. These are states that have no equivalent in the band

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structure of the bulk crystal. Surface states are present at the surfaces of all matters. On metallic surfaces, they are known to lead to a surface dipole which contributes to the work function of the metal surface. On semiconductors, the presence of surface states in the band gap is known to "pin" the Fermi level position of the semiconductor. An important aspect of the surface states is the formation of the surface dipole, which directly affect the electron affinity of the semiconductor. The magnitude of a surface dipole has to do with the entire spatial distribution of charge. The surface states at MS interfaces leads to a weak dependence of the Schottky barrier height on the work function. The ability to control the magnitude of this barrier height is crucial for the advancement of future electronic devices to higher functionality and smaller physical dimensions. An approach involves the insertion of an interface layer between the semiconductor and the metal, in order to obtain stable the Schottky barrier height. This has been accomplished by the introduction of a very thin layer, typically sub-monolayer to a few monolayers, before the metal deposition. It is known that, with the presence an interface layer, the semiconductor electron affinity is significantly increased due to the positive dipole formed between the interface layer and semiconductors. A detailed study of the dependence on the chemical specificity of the interface layer may reveal the fundamental Schottky barrier height mechanism directly [1–5].

The optical, electrical and structural properties of thin films have been extensively studied over the past few years because their characteristic behavior is important to define their potential use in technological areas. Among thin film materials, chalcogenide thin films have attracted much attention due to their large area deposition capabilities and the possibility of depositing them on a variety of surfaces [13]. Copper is stable in media and resists high temperatures. These inherent material properties make copper one of the most important materials for industrial applications. Nowadays, copper based thin films make up a group of highly demanded materials. One of these is copper sulfur (CuS) thin films. CuS thin films have chemical stability, a high absorbent coefficient, high refractive index, and transparence in the visible IR range [14]. It is well known that these properties are strongly dependent on the method used to obtain the thin films. CuS thin films can be grown on a large number of chemical methods on the semiconductor and other substrates [15]. Among them, SILAR is a relatively new and layer-wise chemical deposition technique. It is distinguished for such merits as the layer-by-layer growing feature and the separate precursor of anionic and cationic solutions. SILAR has been widely used to deposit chalcogenide films (CdS, ZnS, CuS, CuSe, ZnSe, etc.), multilayer and epitaxial films since it has been firstly reported by Nicolau in 1985 [16]. However, despite of considerable efforts in this field including the adoption of complexing agent for precursors [17,18] and the reduction of the rinsing time [19,20], the slow growth rate for almost all kinds of films has still been the major disadvantage of SILAR, which limits its application in semiconductor industry.

As an III–V compound semiconductor material, GaAs has been extensively used in high-speed electronic and optoelectronic devices [21–26]. Therefore, the detailed properties of GaAs diodes with different Schottky contact metals (Au, Cu, Ni, Co, Ag and Pt) have been also widely investigated [21–26]. Yet, no report has ever been found regarding the time-dependent of characteristics of Cu/CuS/n-GaAs/In diodes produced by SILAR method in alternative device applications. Due to the issues of barrier modification and stability, diodes with interfacial layer becomes more and more important as a new alternative device and has been employed in electronic industry. In the present study, Cu/CuS/n-GaAs/In Schottky barrier diodes have been prepared directly on n-GaAs semiconductor by the SILAR method. After the device fabrication, its performance and stability depending on time is significant in the device manufacturing. In our previous study [15], the effects of ageing on the electrical characteristics of Cd/CdS/n-Si/Au–Sb structure deposited by SILAR method have been investigated. As part of the same project, in the present study n-GaAs semiconductor has been used as substrate and electrical characteristics of Cu/CuS/n-GaAs/In have been differently evaluated. Therefore, the purpose of this paper is to characterize how the characteristic parameters such as barrier height, ideality factor, series resistance, interface state density distribution and rectifying ratio of Cu/CuS/n-GaAs/In structure have changed with increasing ageing time.

2. Experimental

The Cu/CuS/n-GaAs/In structure used in this study were fabricated using n-type single crystal GaAs wafer with (100) surface orientation and $2.5 \times 10^{17}\,cm^{-3}$ carrier concentration. Before making ohmic contact, the n-GaAs wafer was dipped in $5H_2SO_4 + H_2O_2 + H_2O$ solution for 1.0 min to remove surface damage layer and undesirable impurities, then in a solution of $H_2O + HCl$, then followed by a rinse in deionized water of 18 MΩ.

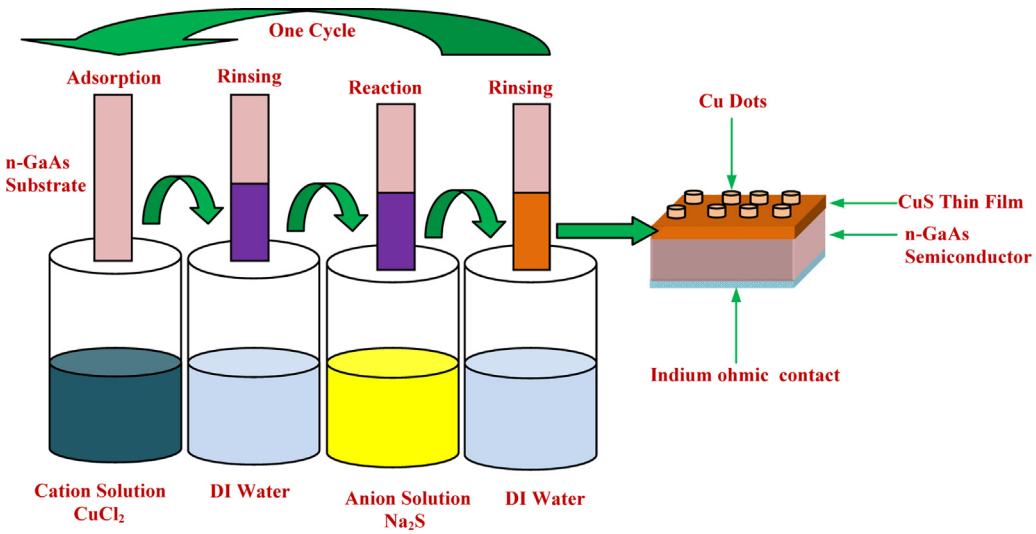

Fig. 1. The processing stage of the SILAR method and schematic cross-section of the fabricated device.

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