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Combinatorial screening of work functions in Ta–C–N/HfO_2/Si advanced gate stacks

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This paper reports a comprehensive investigation into the effects of the C and N contents and temperature anneals on the electrical characteristics of Ta–C–N/HfO_2/Si advanced gate stacks (equivalent oxide thicknesses of ~1.0–1.6 nm) using a combinatorial methodology. The work functions (Φ_m) of Ta–C–N, with higher C and N, can be tuned up to ~5.1 eV after 900 °C anneals, suggesting a promising p-type gate metal for complementary metal–oxide semiconductor applications.

Keywords: Sputtering; Refractory metals; Thin films; Electrical properties; Combinatorial methodology

Continued Moore's law scaling of integrated circuit devices has given rise to gate stack problems, such as high leakage current density (J_L) in SiO_2 dielectrics and depletion in polycrystalline silicon (poly Si) metal gates [1–4]. There has thus been much research on advanced materials to replace SiO_2 and poly Si with high-dielectric-constant (κ) gate dielectrics and metal gate electrodes, respectively. Numerous dielectrics, such as HfO_2 and Hf–Si–O, have been identified as promising candidates to replace SiO_2 [3,5]. However, the search for suitable metal gate electrodes is not as advanced [6].

Ta–C–N films possess several attractive properties, such as tunable work functions (Φ_m), high conductivity and high thermal stability, which make them good candidates as metal electrodes for advanced gate stacks [7–9]. For high-performance or advanced multigate complementary–metal–oxide–semiconductor (CMOS) devices, the Φ_m of metal gate electrodes must be controlled near the conduction band (E_C)/valence band (E_V) or in the bandgap of Si [10]. Either application requires the accurate tuning of Φ_m to reduce the threshold voltage (V_{th}) to minimize power consumption. In addition, an equivalent oxide thickness (EOT) of gate stacks of $\leqslant$1 nm is expected for future advanced logic technology applications [11].

Ta–C–N represents a large composition parameter space, the Φ_m of which is a function of its stoichiometry and can also be tuned by the properties of an underlying dielectric [9,12]. Therefore, a comprehensive determination of the Φ_m of Ta–C–N deposited on a gate dielectric (EOT $\leqslant$ 1 nm) is not trivial. Combinatorial methodology enables efficient generation of a wide and uniform set of samples, and thus allows rapid screening [13–15]. In this paper, we use this technology to rapidly and systematically explore the influence of the C and N contents and temperature anneals on Φ_m of Ta–C–N gate metal electrodes on the dielectrics (HfO_2/Si (~1 nm $\leqslant$ EOT $\leqslant$ ~1.6 nm)) and compare the result with that of the Ta–C–N/HfO_2/SiO_2/Si gate stack.

Ta–C–N thin film composition spreads ("libraries"), about 50 nm thick, were fabricated at room temperature in a radio-frequency reactive magnetron sputtering system.[1] Figure 1(a) is a top view of the metal–oxide–semi-

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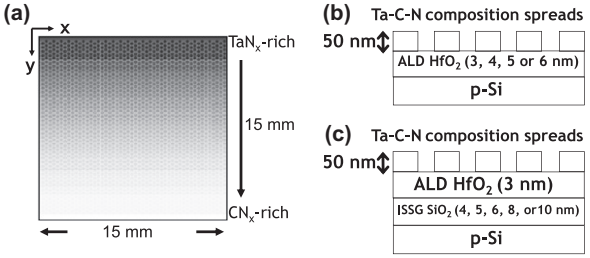

Figure 1. Schematic drawing of the library: (a) top view of a library with hundreds of MOSCAPS; (b, c) side views of Ta–C–N/HfO_2/Si and Ta–C–N/HfO_2/SiO_2/Si capacitor structures.

conductor capacitor (MOSCAP) layout of a typical library. Each library sample was 15 mm × 15 mm in size, and contained a 40 × 60 array of MOSCAPs. A stainless steel shadow mask with hundreds of openings (150 μm diameter, 500 μm apart) was used to make in situ MOSCAPs. Each dot represents a MOSCAP, and the gate electrode composition is continuously changing along the *y*-direction, as indicated in the figure using a false fading-out color from TaN_x-rich to CN_x-rich, whereas it is approximately constant along the *x*-direction. For systemically studying the effect of the C and N content and the interfacial SiO_2 on extraction of Φ_m, several identical Ta–C–N gate electrode library films were deposited on different dielectric stacks: HfO_2(ALD, 3, 4, 5, 6 nm)/Si stacks (Fig. 1(b)) and-HfO_2(ALD, 3 nm)/SiO_2(ISSG, 4, 5, 6, 8 or 10 nm)/Si stacks (Fig. 1(c)). All libraries were subjected to a forming gas anneal (90% N_2 and 10% H_2) at 400 °C for 30 min to minimize interface state density (D_{it}). Details of the library processing can be found elsewhere [16,17]. Rapid thermal anneals (RTAs) at 900 and 950 °C for 10 s were implemented to determine the thermal stability of the Ta–C–N/HfO_2/Si and Ta–C–N/HfO_2/SiO_2/Si gate stacks.

High-resolution transmission electron microscopy (HRTEM) was employed to examine the interfaces in the multilayered gate stack structures. Electron energy loss spectroscopy (EELS) data was recorded using a post-column energy filter in a configuration that yields a collection of spatially resolved spectra across the layer stack (i.e. a spectrum-line). Other analyses for the libraries, such as composition and phase structure, have been published elsewhere [18].

A semi-automatic probe station (Summit 12000B-AP, Cascade Microtech, Inc.)[1] was programmed to measure several hundred MOSCAPs automatically on each library sample. An inductance–capacitance–resistance (LCR) meter, with a parallel resistance–capacitance circuit mode and an alternating current modulation signal level set at 50 mV, was used to measure the capacitance–voltage (C–V) characteristics. To avoid series resistance, a frequency of 1 kHz was used. The measured C–V curves were fitted using a standard program [19] to extract the EOT and flat-band voltage (V_{fb}), which allows the extraction of Φ_m [16].

Figure 2 shows representative HRTEM images, and the EELS spectra of the Ta–C–N/HfO_2(3 nm)/SiO_2(5 nm)/Si sample, recorded near the middle of the library (~$Ta_{0.59}C_{0.25}N_{0.16}$), after forming gas annealing

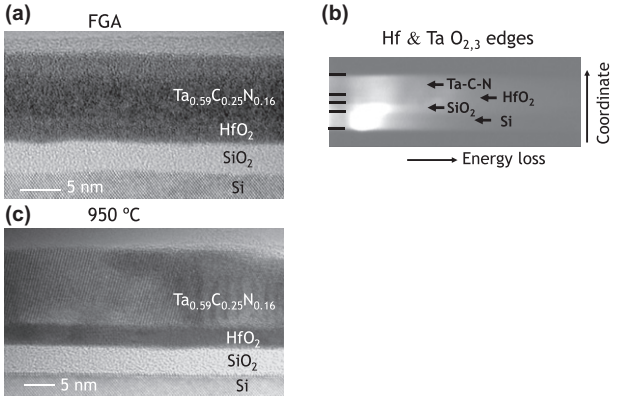

Figure 2. HRTEM and EELS spectrum-line images recorded close to the middle of Ta–C–N/HfO_2(3 nm)/SiO_2(5 nm)/Si, i.e. ~$Ta_{0.59}C_{0.25}N_{0.16}$. (a) HRTEM images after FGA; (b) EELS spectrum-line images after FGA; (c) HRTEM images after a 950 °C RTA.

(FGA) and 950 °C RTA. Additional HRTEM images have been published elsewhere [18]. As shown in Figure 2(a), after FGA, the Ta–C–N/HfO_2 and HfO_2/SiO_2 interfaces remain relatively sharp. The HfO_2 layer is largely amorphous, with only a few occasional crystallites visible in the image, whereas the Ta–C–N layer exhibits some crystallinity. EELS spectrum lines (Fig. 2(b)) for each constituent layer exhibit chemically sharp interfaces (Hf and Ta $O_{2,3}$ core edges), suggesting that no significant interfacial interactions occurred after FGA. As seen in Figure 2(c), after 950 °C RTA, both the Ta–C–N and HfO_2 layers are fully crystallized. EELS spectra from this sample also confirm a lack of significant chemical interactions across the interfaces, but reveal pronounced oxidation of the Ta–C–N layer (not shown). Oxidation of the Ta–C–N layer affects the electrical properties of the gate stacks, as will be discussed later.

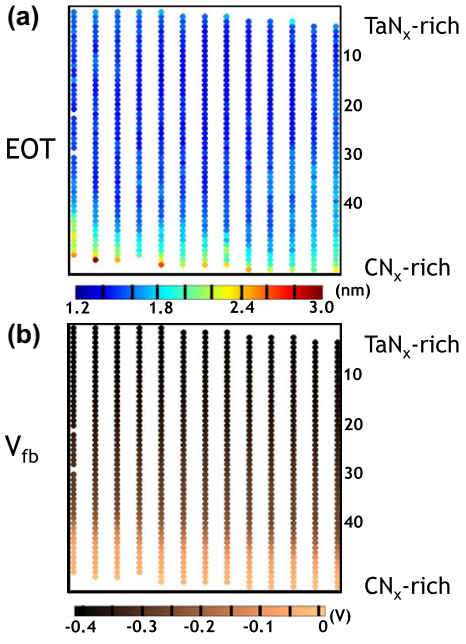

Figure 3. EOT and V_{fb} maps from Ta–C–N/HfO_2(4 nm)/Si library after 900 °C: (a) extracted EOT map; (b) extracted V_{fb} map.