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Prevention of electromigration-induced Cu pad dissolution by using a high electromigration-resistance ternary Cu–Ni–Sn layer

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Abstract

Electromigration-induced Cu dissolution occurred at serious levels on the Cu pad under 10^4 A/cm^2 current-stressing for 20 h at 160 °C. A high electromigration-resistance $(Cu,Ni)_6Sn_5$ layer, which converted from a thin Ni layer on the Cu pad, effectively prevented the Cu pad from dissolving into the pure Sn bump under 10^4 A/cm^2 current-stressing for 30 h at 160 °C.

Keyword: Soldering

1. Introduction

Flip-chip technology has been successfully used for the chip-level assembly of central processing units (CPUs) for decades [1,2]. As the speed and functionality of CPUs continuously increases, a high density of flip-chip I/O (input/output) counts is required. To accommodate such a high density of I/O counts, the size of the flip-chip solder bumps has to shrink. By 2007, the size of flip-chip solder bumps will be approaching 50 μm, and hence the current density in flip-chip solder bumps will dramatically increase to over 10^4 A/cm^2 [1]. Under such a high current density, the electromigration (EM) phenomenon would become a serious threat to the reliability of flip-chip solder bumps.

Two EM failure modes have been reported. The first is the voiding at the cathode side of flip-chip solder joints. Yeh reported that serious voiding occurred at the solder/compound interface of the cathode side after 600 h current stressing under a current density of 10^4 A/cm^2 at 152 °C [3]. Voiding at the solder/compound interface was caused by the net mass transportation of Pb and Sn atoms toward the anode side due to EM. As the voiding area expands with stressing time, the effective resistance across the flip-chip joint would increase quickly and lead to the failure of the flip-chip solder bumps. The second EM failure mode is the EM-induced dissolution of the Cu metal bond pad or Cu trace lines. Kao found that a Cu metal bond pad dissolved into flip-chip SnPb solder bumps under a current stressing of 10^4 A/cm^2 at 100 °C for 45 min [4]. Once the Cu pad completely dissolved into the flip-chip solder bumps, the mechanical reliability of the flip-chip solder joint becomes an issue.

There is now a trend to using Pb-free solders in the electronic packaging industry. SnPb flip-chip bumps will eventually be replaced by Sn-rich Pb-free solders. Some researchers have studied the EM behavior of the promising Sn-rich Pb-free solders, such as SnAg, SnCu, and SnAgCu [5–7]. They found that those Sn-rich Pb-free solders exhibited much better EM resistance than eutectic SnPb solders. Therefore, the first EM failure mode mentioned above, i.e., voiding at the cathode interface, would be alleviated by using Sn-rich solders in flip-chip solder bumps. However, Sn-rich solders all contain over 95 wt.% of Sn, and have

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much higher Cu solubility than SnPb [8]. Therefore, serious EM-induced Cu dissolution would be expected in Pb-free Sn-rich solder bumps. In this study, we investigated the EM-induced Cu dissolution in Sn-rich solders and an EM barrier layer for the Cu bond pad.

2. Experimental

For simplicity, we used pure Sn flip-chip solder bump for the EM-induced Cu dissolution study. 99.99% purity of Sn wire purchased from Alpha Corporation was used to prepare pure Sn solder balls. 0.1 mg pure Sn pieces were cut off from the Sn wire and those cut-off Sn pieces were reflowed in the flux ambient to form spherical Sn solder balls. The diameter of the pure Sn balls was about 200 μm. Then, the Sn solder ball was reflowed on a 1×1 cm Cu foil with 25 μm thickness. By controlling the reflow time, 25 s, and the reflow temperature, 250 °C, a semispherical solder bump could be achieved on the Cu foil, as illustrated in Fig. 1(a). The finished samples (Sn solder bump on Cu foil) were loaded into the set-up of the EM test, which is illustrated in Fig. 1(b). A stainless metal frame was placed on a hot plate, which is electrically isolated from the hot plate by inserting glass slides between the stainless frame and the hot plate. A Cu rod was placed on the top of the pre-flattened Sn solder bump to serve as the top electrode. The hot plate was controlled at a constant temperature of 160 °C. Then, a constant current density of 10^4 A/cm^2 was applied in the Sn solder bump by a power supply, for two different stressing times: 20 and 30 h. Current-stressed samples were mounted into the epoxy resin for scanning electron microscopy (SEM) cross-sectional study. First, a diamond saw was used to section samples through the solder bump. Then, samples were polished with sand papers and finished with polishing clothes down to 0.1 μm alumina powders. After polishing, the samples were etched by the dilute HCl solution (95% C_2H_5OH + 5% HCl) to reveal the morphology of the interface for SEM examination.

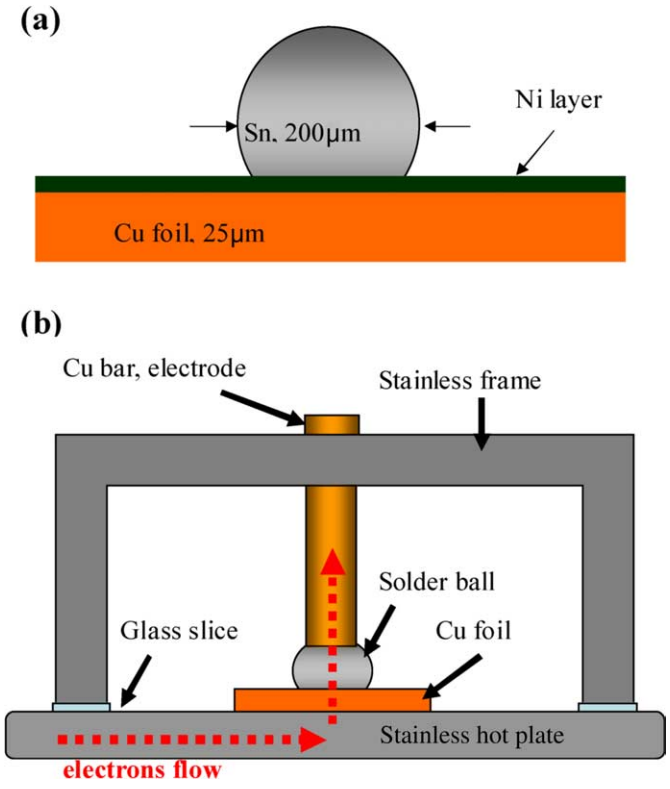

Fig. 1. (a) Drum-shaped Sn bump on the Cu foil; (b) schematics of EM-test set-up.

3. Results and discussion

Fig. 2(a) and (b) are the cross-sectional images of Sn bumps on Cu foils after 20 and 30 h current stressing, respectively. As seen in Fig. 2(a), we can observe that the Cu foil was significantly consumed and a relatively thick Cu–Sn compound layer formed at the interface after 20 h stressing time. It implies that the Cu atoms in the Cu foil were electro-stressed into the Sn bump via the interfacial Cu–Sn compound layer. Then, the dissolved Cu atoms reacted with

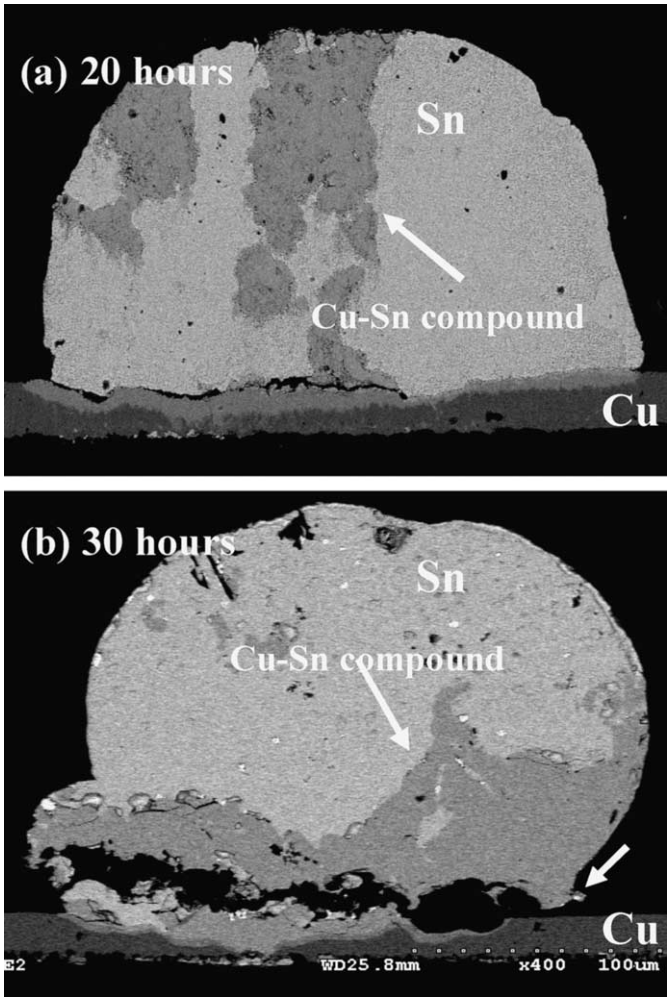

Fig. 2. SEM cross-sectional images of Sn bumps on Cu foils after (a) 20 h and (b) 30 h current stressing.