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ScienceDirect

Solid State Sciences 10 (2008) 1222–1227

Solid State Sciences

www.elsevier.com/locate/ssscie

Mechanical stress sensor of (n^+)nanocrystalline/(p^+)crystalline Si heterojunction

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Received 21 September 2007; received in revised form 26 October 2007; accepted 6 November 2007
Available online 21 November 2007

Abstract

A heterojunction of heavy phosphorus doped hydrogenated nanocrystalline Si film with heavy doped p-type crystalline Si wafer was prepared and measured to investigate mechanical stress effect on electronic characteristics. The yielded structure was demonstrated as a semiconductor backward diode according to current–voltage relation measurements, from where the absence of sequent resonance tunneling in conduction was also interpreted. Mechanical stress effect on electronic characteristics of the operated diode can be mainly ascribed to stress-induced bulk defect states instead of interface states, however, applied stress doesn't change conduction mechanism in this study. Soft breakdown in stressed junction was illustrated. Before breakdown the reverse operated current shows good linear dependence on applied stress with an effectual method of transforming mechanical signal to electronic one, which reveals the fabricated device as potential mechanical stress sensor in the future.

PACS: 71.55.Cn; 73.40.-c; 73.61.-r; 73.61.Tm; 68.35.Dv

Keywords: Nanocrystalline Si; Heterojunction; Stress sensor; Defect state

1. Introduction

Si crystalline heterojunction (HJ) diodes and tunnel diodes used for pressure sensors have widely been studied in terms of material and device physics, design and fabrication technology and applications for decades [1,2]. Hydrostatic pressure effect on p–n junction performances due to variation of semiconductor energy band gap while anisotropic stress effect on current–voltage ($I-V$) characteristics owing to lattice defects were denoted whereas stress effect on reverse $I-V$ properties was not obtained. However, low sensitivity and poor linearity between output voltage and stress were indicated in Si conventional diodes. Although silicon tunnel diodes indicated higher stress sensitivity and better linearity when they were operated in positive resistance region of $I-V$ curves, its applications were also limited since suffering the difficulty for selecting a shunt resistance and operating the diode properly. This case was also encountered by the hydrogenated amorphous silicon p-i-n HJ [3]. With developing of nanotechnology, hydrogenated nanocrystalline Si (nc-Si:H) film as a kind of multiphase mixed material, of which is comprised of Si nanocrystals and hydrogenated amorphous silicon (a-Si:H) matrices, has been prepared to investigate its interesting physical properties and applications such as sequent resonant tunnel diode and photovoltaic cell and so on [4–6]. In our recent work, a backward diode of (n^+)nc-Si:H/(p^+)c-Si was fabricated while electronic conduction mechanisms were investigated [7]. This further inspires us to explore stress effect on electronic characteristics and facilitate sensor applications for these HJs.

Herein, a large area with 3.14 mm^2 HJ of electrode/(n^+)nc-Si:H/(p^+)c-Si/electrode was deposited using same method and conditions as the previous one with small junction area [7]. Subsequently, mechanical force was loaded on the fabricated HJ. After electrical measurements and analysis, results reveal that the produced structure can be regarded as a semiconductor backward diode. Stress effect on $I-V$ and capacitance–voltage ($C-V$) characteristics of this unit was interpreted by

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1293-2558/$ - see front matter
doi:10.1016/j.solidstatesciences.2007.11.011

stress-induced defect states, which differs from another report [8] due to different doping level and applied stress method.

2. Experimental details

Around 100 μm thick single facet polished p^+-type (100) silicon wafer with an average resistivity of 0.0006 $\Omega\,cm^{-1}$ ($N_A \approx 2.4 \times 10^{20}\,cm^{-3}$) was used as substrate. The (n^+)nc-Si:H/(p^+)c-Si structure was prepared with a planer process. Firstly, a 3 μm thick SiO_2 layer was prepared by thermal oxidation on substrate at 1293 K. Then the SiO_2 layer was etched and patterned by photolighography to make an array of circular holes ($1 \times 1 \times \pi$ mm^2). Silane SiH_4 was strongly diluted in hydrogen H_2 with dilution ratio of 1.0 vol% (namely, SiH_4/H_2 in volume percentage) to use as reactant gas, while phosphine PH_3 was doped into silane SiH_4 with doping ratio 10.0 vol% to form mixed reactant source gas. It is emphasized that the dilution ratio (R_d) and doping ratio were adopted herein since they were also used to successfully fabricate similar units in our previous work [5,7]. Then, a fresh phosphorus doped nc-Si:H film was deposited on the patterned substrate by using mixed reactant source gas. The deposition was operated in a capacitively coupled radio-frequency (RF of 13.56 MHz) plasma enhanced chemical vapor deposition (PECVD) system aided with direct current (DC) bias stimulation. The other process parameters were set as following: substrate temperature 523 ± 1 K, RF power density $0.6 \pm 0.05\,W\,cm^{-2}$, reactant gas pressure 100 ± 5 Pa and a negative bias -200 ± 2 V applied to substrate. Subsequently the outer layer of nc-Si:H film in the circular hole was removed by etching and photolithography, preserving about 3 μm thick phosphorus doped nc-Si:H film in hole. The aim for growth thick film is in order to avoid amorphous buffer layer as high potential barrier sandwiching between (p^+)c-Si substrate and (n^+)nc-Si:H film. Further, one can expect that interband tunnel can be emerged form the conducting HJ. On the other hand, it also can prevent cracking and particulate piercing when applied mechanical stress to the junction in later experiments. In addition, using this Si oxide can avoid carrier leak from flank of the fabricated heterojunction. Ultimately, Al and In films as Ohmic contact electrodes were prepared by thermal evaporation on the sides of substrate and nc-Si:H film, respectively.

A high resolution transmission electronic microscope (HRTEM) photo for the cross section of nc-Si:H/c-Si as denoted in Fig. 1 was taken by a transmission electronic microscopy JEM-2010 with operation voltage of 200 kV and resolution of 0.19 nm, from which one can find that inappreciable buffer layer was incubated upon c-Si substrate. In order to investigate mechanical stress sensitivity on electronic characteristics of the prepared device, a compressive stress-application apparatus presented in Fig. 2 was set up. Firstly, an aluminium post (symbol of a in Fig. 2) with a flat butt area of $1 \times 1 \times \pi$ mm^2 was utilized not only to load mechanical stress but also for a lead of top electrode in experiment. Subsequently, two posts with hummocky butt (symbols of b and c in Fig. 2) with different radius were selected in tests, respectively. To ensure good electrical contact between post and electrode,

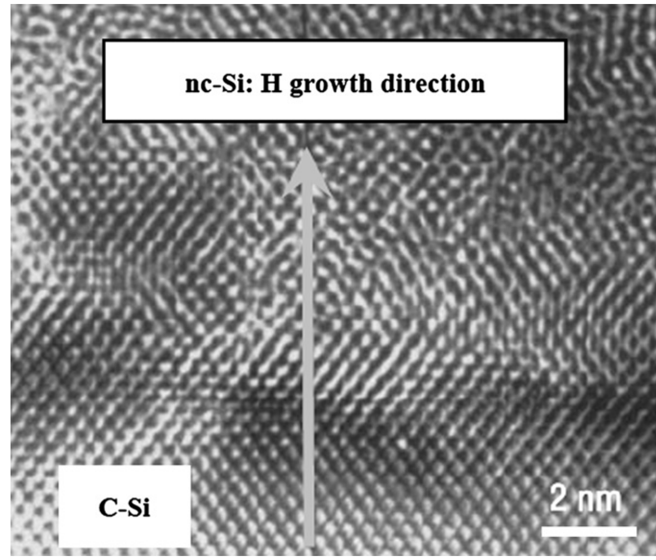

Fig. 1. A high resolution transmission electronic microphotograph (TEM) of the cross section of nc-Si:H/c-Si, which displays invisible buffer layer on c-Si substrate.

some initial force was necessary for measurement. Precise alignment of the post was needed to assure that stress was applied perpendicular to device surface. To obtain repeatable and reliable results, the posts were carefully cleaned and positioned in center of substrate surface of hetrostructure, respectively. The force introduced to apply the mechanical stress in present study was set as 4.9, 9.8, 14.7 and 19.6 N, respectively, from which the range of engendered pressure loaded to present HJ is consistent with that used in literature [1,2] as a consequence of effective comparison. These force values were ever properly selected to detect stress effect on $I-V$ characteristics of polycrystalline diamond film Schottky diodes [9]. Stress-induced $I-V$ performances of the fabricated structure were recorded by a computer-controlled system including HP4140B picoammeter with DC voltage source at room temperature, as depicted in Fig. 3 with the applied force as a parameter. In addition, stress-induced $C-V$ characterizations were measured by a HP4280A precision LCR meter under condition of a DC

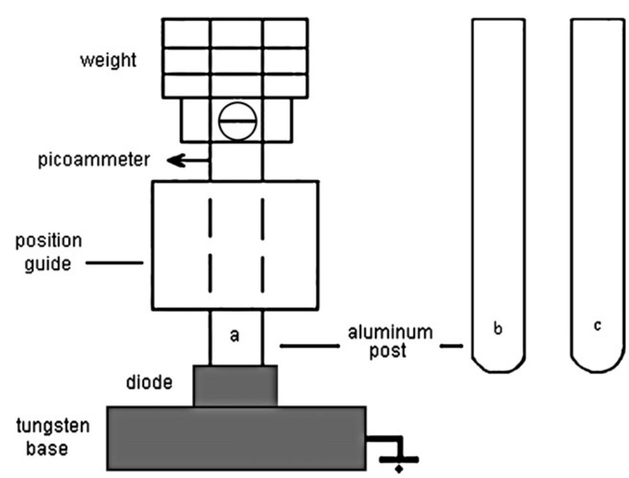

Fig. 2. Schematics of stress applied apparatus.