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Research on fast fault identification method of 10.5 kV/1.5 kA superconducting fault current limiter

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A B S T R A C T

Superconducting fault current limiter (SFCL) is a prospective electric devices connected in series in power grid to limit short-circuit current. A 10.5 kV/1.5 kA 3-phase SFCL with HTS coil of 6.24 mH was developed at IEECAS in China in 2005, which was operated in a local power grid in Hunan province for more than 11,000 h, and integrated lately in a superconducting power substation in Baiyin city in 2011 and is still running safely and reliably. In order to reduce the fault response time and enhance the performance of the SFCL, we analyzed the structure characteristics of the SFCL and discussed the variation of currents and voltages of the HTS coil and the bridge during the fault time. The simulation and tests results of power system validate the feasibility of the fast fault identification method.

1. Introduction

Superconducting fault current limiter (SFCL) is a prospective and developing electric device connected in series in power grid to limit short-circuit current [1]. Lots of experts focus on the bridge type SFCL. It is in 1999 that a 15 kV, 20 kA bridge-type HTS fault current limiter was designed and developed in Los Alamos National Laboratory in USA [2]. The bridge type SFCL was improved to reduce of inductance and current rating of the coil in Japan in 2000 [3]. A 10.5 kV/1.5 kA 3-phase SFCL shown in Fig. 1 was developed at IEECAS in 2005 and integrated in a superconducting power substation in Baiyin, China in 2011. The 3-phase SFCL is still running safely and reliably [4,5] at present. In recent years, the SFCL has been further improved in cryogenic and refrigeration equipment, which reduce the heat losses obviously.

The SFCL was designed in improved bridge-type which employs the bridge-type SFCL and the resistor shunt with IGCT switch as bypass. When a short-circuit fault occurs, the HTS coil can limit the over-current automatically. At same time, the controller can detect the fault signal and control the IGCT to switch off, then the resistor is connected into the line. The fault current is then limited by both the HTS coil and the resistor. The controller detects the fault signal when the current exceeds the given value. But In actual operation, the line current varies greatly from day to night. It is very difficult to detect the fault signal without delay. The HTS coil only limits the rising rate of fault current and the peaks of fault current are difficult to limit. Therefore, it is very significant to achieve the fast fault identification and insert the resistor into the line to limit the fault current timely.

Resonant-type fault current limiter is developed from TPSC (thyristor protected series capacitor), where the short-circuit fault is recognized by the analyzing the instantaneous value characteristic and fast identification criterion of fault current [6]. The paper [7] shows that the short-circuit fault also can be identified by resonant voltage difference.

In order to reduce the fault response time (FRT) and enhance the performance of the SFCL, we analyzed the structure characteristics of the SFCL and discussed the variation of currents and voltages detected from the HTS coil and the rectifier bridge during fault time. Simulation results showed the response time of different methods and gave a quick response method.

2. Working principle

One phase schematic of the SFCL is shown in Fig. 2, which consists of a HTS coil, abridge circuit (diode D1–D4), a HTS coil with protective circuit (Re and De) and a resistor (R) connected with IGCT in parallel. The SFCL has the limiting characteristic both as inductance type and resistance type SFCL.

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Fig. 1. SFCL in superconducting power substation.

In the original design, with the demand of the SFCL running in a real grid, the HTS coil have to withstand a high lightning surge voltage of 75 kV, rated voltage of 10.5 kV, and a high impulse current of 1.5 kA [2]. In order to improve the SFCL, there are two ways can be used to reduce surge voltage and over-current of SFCL:

- MOV (metal oxide varistors) should be connected to SFCL in parallel to reduce the surge voltage.
- FRT should be reduced to avoid the impulse of fault current to destroy devices.

The basic working principle of the SFCL and the characteristic of the fault current have been analyzed in detail [8]. In order to identify the fault as quick as possible, we focused on the fault current impulse to analyze the current rising rate (CRR) during short-circuit fault. As the main limiting device, HTS coil charges and discharges alternately and constantly because the current (i) of the line is AC and the current (i_L) of HTS coil is DC. Consideration of the resistor switching on and off, HTS coil has experienced four stages, in which the CRR varies obviously with different stage.

Once the short-circuit fault occurs, the equivalent impedance of the line is almost inductive, especially the fault occurred in bus. The IGCT is still switched on and the resistor is shunted. If the voltages of diodes and IGCT is omitted.

First stage: when $|i| < i_L$ and The IGCT is still switched on, HTS coil discharges and the resistor is shunted. The voltage of the rectifier bridge u_b is almost zero. The equations of the line are given by

$$\begin{cases} U\cos(\omega t) = L_1 \frac{di}{dt} \\ L\frac{di_L}{dt} = 0 \end{cases} \tag{1}$$

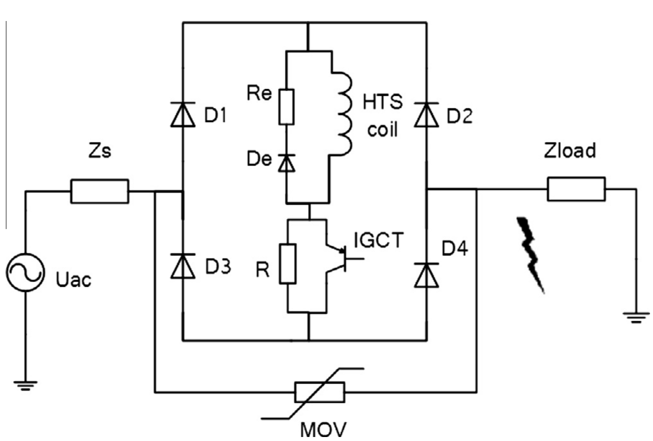

Fig. 2. Schematic of bridge-type SFCL (one phase).

where U is the peak voltage of power supply, L is inductance of HTS coil, and L_1 is the equivalent inductance of the line during fault. i and i_L are the currents of the circuit and HTS coil respectively. The initial fault angle $\theta = \omega t$, which is the angle when the fault start to occur.

There are different variation characteristics between the CRR of the line (di/dt) and of the HTS coil (di_L/dt) as shown below.

$$\begin{cases} \frac{di}{dt} = \frac{U\cos(\omega t)}{L_1} \\ \frac{di_L}{dt} \approx 0 \end{cases} \quad (|i| < i_L) \tag{2}$$

The CRR of the line is determined by the fault time (t) and the inductance (L) of HTS coil. It is also determined by the parameter L_1, which stands for the fault extent of the line. While, the CRR of HTS coil is almost zero because the voltage of the bridge is zero. As a result, the SFCL has no effect to the fault current in this stage.

Second stage: when $|i| \geqslant i_L$ and The IGCT is still switched on, the HTS coil starting to charge and become effective to the fault. The voltage u_b is still not zero. The equations of the line are given by

$$\begin{cases} U\cos(\omega t) = L_1 \frac{di}{dt} + u_b \\ |u_b| = L\frac{di_L}{dt} \end{cases} \tag{3}$$

The relationship of the CRRs are given by

$$\begin{cases} \frac{di}{dt} = \frac{U\cos(\omega t)}{L_1 + L} \\ \frac{di_L}{dt} = \frac{d|i|}{dt} \end{cases} \quad (|i| \geqslant i_L) \tag{4}$$

The CRRs are same because the connection relationship of inductor L_1 and L is equivalent in series. So the CRRs are restricted obviously for the HTS coil is effective to the fault, but the peak of the fault current is difficult to limit.

Third stage: when $|i| < i_L$ and The IGCT is switched off, HTS coil discharges and the resistor is inserted into the line. The voltage of the rectifier bridge u_b is almost zero. The equations of the line are given by

$$\begin{cases} U\cos(\omega t) = L_1 \frac{di}{dt} \\ L\frac{di_L}{dt} + i_L R \approx 0 \end{cases} \tag{5}$$

where u_b stands for the limiting capability of the SFCL. The value of u_b is zero means than the SFCL has no limiting effect on the CRR of the line. The relationship of the CRRs are given by

$$\begin{cases} \frac{di}{dt} = \frac{U\cos(\omega t)}{L_1} \\ \frac{di_L}{dt} = -\frac{R}{L} i_L \end{cases} \quad (|i| < i_L) \tag{6}$$

where the SFCL has no limiting effect on the CRR of the line. While, HTS coil discharges by the resistor and the current i_L is decrease, and the CRR of HTS coil increases negatively for a current loop formed by the resistor and HTS coil through the diodes.

Fourth stage: when $|i| \geqslant i_L$ and The IGCT is switched off, the HTS coil starting to charge and become effective to the fault. The resistor is also effective to fault current. The equation of the line is as shown below.

$$\begin{cases} U\cos(\omega t) = L_1 \frac{di}{dt} + u_b \\ |u_b| = L\frac{di_L}{dt} + i_L R \end{cases} \tag{7}$$

The relationship of the CRRs are given by

$$\begin{cases} \frac{di}{dt} = \frac{U\cos(\omega t) - U_b}{L_1} \\ \frac{di_L}{dt} = \frac{|u_b| - i_L R}{L} \end{cases} \quad (|i| \geqslant i_L) \tag{8}$$