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A Comparative Study of Sinusoidal PWM and Third Harmonic Injected PWM Reference Signal on Five Level Diode Clamp Inverter

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Abstract

This paper present the comparative modulation of Sinusoidal PWM and Third Harmonic Injected PWM Reference signal with carrier signal PD, POD, and APOD on 5 Level Diode Clamp on a R-L load. All of process are simulate with computer program MATLAB/Simulink. The result of simulation has shown value of THD_V line-line output voltage on both SPWM inverter and Third Harmonic Injection modulation inverter with PD carrier signal generate a minimum THD_V.

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Keywords: DC-MLI; SPWM; Harmonic Injected PWM; PD; POD; APOD; THD_V

1. Introduction

Multilevel inverter is a most popular for the industrial and electric power systems, because of it is high performance and low Harmonics. There are various types of Multi-Level Inverters such as Neutral-point clamped (NPC) or Diode Clamped (DC) inverter, Flying capacitor inverter and Cascade inverter. The difference among these kinds is as follow, when level of output voltage of Neutral-point clamped (NPC) or Diode Clamped inverter is

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increased, a number of diodes is also increased accordingly. When level of output voltage of Flying capacitor inverter is increased, a number of capacitor is also increased. It leads into higher cost and more switching losses. Cascaded multilevel inverters have advantages and benefits than the other, because it need no require in balancing capacitors and diodes, in another way it just need a separate DC source for each H-Bridge. [1]

Therefore, in this paper, Diode Clamped Inverter is used for comparative study, especially in carrier based SPWM and HIPWM. However the configurations of their modulation techniques are PD, POD and APOD as shown Fig.1.

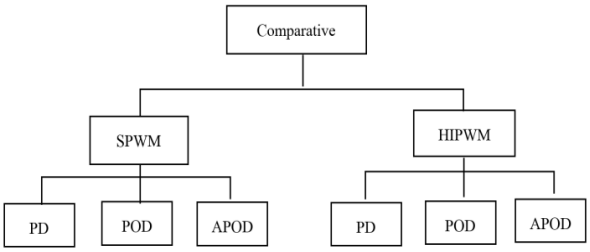

Fig. 1 Structure of the modulation scheme that is used in this paper

2. Background

2.1. Diode Clamped Inverter

The first invention in multilevel converters was called as a neutral point clamped inverter. It was initially proposed of a 3 phase three level inverter. [2]

The main benefits and drawbacks of this topology are:

- The performance of its output waveform is high, especially at fundamental frequency.
- The whole capacitors have to be pre-charged at the beginning of the operation.
- Output voltage level depends on the capacitor voltage. In which, the equality of their capacitor is needed in order to keep the balancing of the 3 phase output voltage.

2.2 Reference Signal

SPWM

To generate Sinusoidal PWM signal a sine wave is provided as a reference signal. The frequency of a sine wave is equal to the frequency of the desired output voltage to the modulation of the carrier signal. The switching frequency of carrier signal must be higher than reference signal frequency as triple-N number. When both signals are modulated, it will generate the signal pulse for the switching devices for the inverter [3] as shown in Fig.2