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Combined impact of heterogeneous lifetime and gettering on solar cell performance

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Abstract

We couple numerical process and device simulations to provide a framework for understanding the combined effects of as-grown wafer impurity distribution, processing parameters, and solar cell architecture. For this study, we added the Impurity-to-Efficiency simulator to Synopsys' Sentaurus Process software using the Alagator Scripting Language. Our results quantify how advanced processing can eliminate differences in efficiency due to different as-grown impurity concentrations and due to different area fractions of defective wafer regions. We identify combinations of as-grown impurity distributions and process parameters that produce solar cells limited by point defects and those that are limited by precipitated impurities. Gettering targeted at either point defect or precipitate reduction can then be designed and applied to increase cell efficiency. We also visualize the post-processing iron and total recombination distributions in 2D maps of the wafer cross-section. PV researchers and companies can input their initial iron distributions and processing parameters into our software and couple the resulting process simulation results with a solar cell device design of interest to conduct their own analyses. The Alagator scripts we developed are freely available online at http://pv.mit.edu/impurity-to-efficiency-i2e-simulator-for-sentaurus-tcad/.

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1. Introduction

Multicrystalline silicon (mc-Si) wafer quality varies widely. Total impurity concentrations and the area fraction of high defect density [1-3] both impact solar cell performance. Poorly performing areas are disproportionately detrimental [4], and wafers with higher defect concentrations are not sufficiently remediated by standard gettering [5]. Thus, treating all mc-Si wafers with the same process results in lower average efficiencies with a wider standard deviation [6]. Sorting wafers by quality, defined by the area fraction of high dislocation density, with inline photoluminescence imaging can enable better statistical process control and smaller standard deviations in cell performance [1-3]. A fast, 1D gettering model, the Impurity-to-Efficiency (I2E) Simulator [7] is a powerful tool for process optimization [8,9], but it does not capture 2D effects. Additionally, 2D simulations enable analysis of gettering in advanced cell architectures including Passivated Emitter and Rear Cell (PERC) and Interdigitated Back Contact. For this study, we developed a 2D version of the I2E Simulator for use with Synopsys, Inc.'s Sentaurus TCAD simulation software. We couple 2D phosphorus diffusion gettering (PDG) and solar cell device simulations to define effective gettering of mc-Si wafers for two different wafer sets. Wafers in Scenario A have different total iron concentrations [Fe_0] but the same area fraction of dislocation-rich grains (*e.g.* from different ingot heights but similar crystal structure). Wafers in Scenario B have different area fractions of dislocation-rich grains but the same [Fe_0] (*e.g.* same ingot height but from different bricks). Our results present a pathway for manufacturers to identify optimal processing for wafers sorted by total impurity content and by the area fraction of defective regions.

2. Simulation models

To simulate in 2D the redistribution of iron impurities during solar cell processing, we added the kinetics and thermodynamics of precipitates, interstitials, and their redistribution during phosphorus diffusion gettering as defined in the Impurity-to-Efficiency Simulator [7,10] to Synopsys' Sentaurus Process *via* the Alagator Scripting Language [11]. The process simulation results are passed to Sentaurus Device [12] to simulate the performance of a PERC solar cell architecture. The wafer is *p*-type, with a resistivity of 2 Ω-cm and a thickness of 180 μm. A distance of 1.2 mm is assumed between two front grid finger contacts, while local rear contacts are 600 μm apart. Further details of the device architecture and simulation input parameters can be found in [13,14]. We explicitly calculate recombination due to interstitial iron (Fe_i) and the carrier lifetimes associated with iron-silicide precipitates (Fe_p), and we assume a uniform 2 ms background lifetime to account for other homogeneously distributed recombination sources. The rest of the model parameters are taken from well-known physical models or fitting to experimental values.

3. Simulation scenarios

We simulated three PDG time-temperature (*t*-*T*) profiles, each tailored to optimize iron removal for different [Fe_0]. All three profiles consisted of a 30-minute isothermal phosphorus diffusion step at 840°C followed by a linear cool to 500°C. The cooling rate was varied such that the cool took 5, 20, or 100 minutes, with longer cooling times tailored to higher impurity contents. To analyse the effect of different post-processing iron distributions on efficiency, we simulated two different material Scenarios. In both Scenarios, we simulate a 600 μm-wide simulation domain with three wafer regions: (1) a lower impurity content "cleaner" grain, consistent with low dislocation density; (2) a 6 μm-wide grain boundary (GB); and (3) a higher impurity content "dirtier" grain, consistent with high dislocation density. We assumed spherical iron-silicide precipitates with an initial radius of 30 nm [8]. From the initial precipitate radius and the initial [Fe_p] in each wafer region, we calculated a spatial precipitate density, which remains constant as the simulated process proceeds. The precipitate densities vary several orders of magnitude across the three wafer regions.

In Scenario A (Fig. 1 (left)), the fraction of the wafer that was "cleaner" (low dislocation density) was fixed at 70%, and the as-grown total wafer-level iron concentration, [Fe_0], was varied between 4×10^{12} cm^{-3} (middle of a mc-Si ingot) and 1×10^{15} cm^{-3} (top of a mc-Si ingot). [Fe_0] as a function ingot height was calculated as in [8], and these Fe concentrations are typical for a cast mc-Si ingot [8]. The average [Fe_i] for the chosen impurity levels varies between 5×10^{10} cm^{-3} and 7.5×10^{12} cm^{-3} [8], so we defined the "cleaner" grain as having [Fe_i] equal to half the