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Industrial Process Leading to 19.8% on N-Type Cz Silicon

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Abstract

High efficiencies have been demonstrated on n-type solar cells thanks to advanced passivation layers and metallisation techniques. In this paper we present the latest results obtained with our bifacial cell structure, using BCl_3 diffusion for emitter formation, thermal SiO_2 passivation and screen-printing metallisation. By continuously improving front side contact quality and reducing substrate bulk lifetime degradation we were able to steadily increase the efficiency of our solar cells from 18.8% to 19.8% on large area c-Si wafers. A first PV module of 21 cells exhibiting an output power of 92 W_p was fabricated.

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Keywords: Solar cell; n-type silicon; boron diffusion; high efficiency

1. Introduction

The highest efficiencies obtained so far on industrial silicon solar devices involve technologies implemented on n-type substrates [1, 2]. One way to reduce solar energy cost ($/W) is to elaborate solar cells reaching higher efficiencies by developing cost-effective processes using Cz Si(n) substrates [3, 4]. The cell architecture considered here is a bifacial n-type PERT (Passivated Emitter Rear Totally diffused) structure. The PERT structure developed at INES includes blanket boron emitter on the front side and blanket phosphorus Back Surface Field on the rear. BCl_3 diffusion is used for emitter diffusion while conventional $POCl_3$ diffusion is used for elaborating the BSF. Emitter and BSF passivation are ensured by

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a SiO_2/SiN stack. Silver based screen-printing pastes are used for both front and rear side metallisation. The efficiencies obtained on medium area c-Si(n) wafers (148.6 cm²) with our baseline process were already presented in details (see [5]). When implementing the process on large area wafers (239 cm²) we were able to reach a best efficiency of 18.8% (see Table 1). Nevertheless the scaling up of our process highlighted significant limitations in terms of fill factor (FF) and open circuit voltage (V_{oc}) while the short-circuit current was not impacted. The present paper focuses on solutions investigated to rule out the V_{oc} and FF limitations.

Table 1. Average and best n-type PERT solar cell parameters under STC (1000W/m²; 25°C) before optimisation

Cell area: 239cm²	J_{sc} (*mA/cm²*)	V_{oc} (*mV*)	FF (*%*)	PFF (*%*)	η (*%*)
Average (12 cells)	37.8	628.3	77.7	81.8	18.5
Best	38.0	631.3	78.2	81.9	18.8

2. Experimental

2.1. Promoting a high end-of-process bulk lifetime

Silicon solar cell efficiency is strongly depending on substrate intrinsic electrical properties. As previously mentioned, the processing of n-type PERT cells involves two high temperature steps (boron diffusion and thermal oxidation, see Fig. 1a) which open the door to possible degradations of the silicon substrate (by detrimental effects of oxygen precipitation, BRL growth during boron diffusion [6], and improper ramping conditions during oxidation [7]). In this context, the proper tuning of the different thermal treatments is crucial to preserve silicon bulk quality all along the process-flow. A specific study was devoted to this tuning. Czochralski c-Si (n) wafers underwent n-type PERT processing steps leading to $p^+/n/p^+$ samples passivated by SiO_2/SiN stacks. Different conditions of BCl_3 diffusion and thermal oxidation were tested. In order to evaluate the impact of processing steps on bulk properties, the passivating stacks and doped regions were removed chemically and the recovered substrates were coated by our referent passivating (Si-rich SiN) layer. These samples are referred to as *'PERT substrates'* in the rest of the paper. The effective lifetime of charge carriers in these samples is assumed to be mainly limited by bulk recombination, and measured for an injection level of 10^{14} cm^{-3} using QSSPC setup. The averaged results (three samples per test) are presented in Fig. 1. The first tests (1 to 4) consisted in reducing the thermal budget of the BCl_3 diffusion, and lead to a drastic improvement of effective lifetime (~800 µs). Then the BCl_3 recipe optimisation (driven by the will to reduce the BRL thickness and to improve its homogeneity at wafer scale) allowed us to keep the lifetime superior to 1000 µs along the process. Eventually the tuning of the oxidation recipe (mainly the ramping conditions) made it possible to reach lifetimes above 1200 µs.