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Structural and electrical characteristics of a high-k Lu_2O_3 charge trapping layer for nonvolatile memory application

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ABSTRACT

In this article, we reported a metal-oxide-high-k-oxide-silicon (MOHOS)-type memory structure fabricating a high-k Lu_2O_3 film as a charge trapping layer for flash memory applications. X-ray diffraction and X-ray photoelectron spectroscopy revealed the structural and chemical features of these films after they had been subjected to annealing at various temperatures. The high-k Lu_2O_3 MOHOS-type devices annealed at 800 °C exhibited a larger threshold voltage shift (memory window of ~2.93 V operated at V_g = 9 V at 1 s) and better data retention (charge loss of ~18% measured time up to 10^4 s) than that had been subjected to other annealing conditions. This result suggests the higher probability for trapping of the charge carrier due to the formation of the crystallized Lu_2O_3 with a high dielectric constant of 12.8.

1. Introduction

Metal-oxide-nitride-oxide-Si (MONOS) type flash memory devices have been employed for a new generation of nonvolatile memory in preference to a conventional poly-Si floating-gate memory [1,2]. However, a major challenge for such devices is achieving simultaneously high program/erase (P/E) speed and good data retention time, because the tunneling current through the thin tunneling oxide film critically affects the electrical characteristics [3]. The data retention becomes even worse at elevated temperatures, because the trap energy in Si_3N_4 is much shallower compared to the conventional deep-energy poly-Si floating-gate memory [1]. To overcome this problem, various high-k materials, such as HfO_2, ZrO_2, Al_2O_3, Ta_2O_5, and Y_2O_3 [4–8], have recently attracted much attention as a charge trapping layer to replace the silicon nitride. However, the flash device with trapping layer of HfO_2 has serious problem in retention characteristics and that with Al_2O_3 layer has the problem of low operation speed.

Rare-earth oxide films have been extensively investigated as high-k gate dielectrics to replace silicon oxide in complementary metal-oxide-semiconductor (CMOS) devices due to their promising thermal, chemical, and electrical properties [9]. Among them, Lu_2O_3 (lutetia) thin film is proposed for high-k gate insulator applications because of its high dielectric constant [12,13], large bandgap, good hygroscopic immunity, and good thermal stability with Si [10]. Darmawan et al. [11] demonstrated that Lu_2O_3 dielectric film deposited by pulsed laser deposition has a high k value of 45. It has been also reported that Lu_2O_3 thin film exhibited a higher lattice energy (−13,871 kJ mol^{-1}), a larger band gap (5.5 eV), and a lower leakage current than other lanthanide oxide thin films [12]. Furthermore, the large conduction- and valence-band offsets at the Lu_2O_3/Si interface are 2.1 and 2.6 eV [13], respectively. However, experimental data related to the charge trapping behavior of lutetia is not clear now. In this study, we proposed a metal-oxide-high-k-oxide-silicon (MOHOS)-type memory device incorporating a high-k Lu_2O_3 film as the charge trapping layer. We used X-ray diffraction (XRD) and X-ray photoelectron spectroscopy (XPS) to characterize the film structures and compositions of the lutetia dielectrics after post-deposition annealing (PDA) at various temperatures, respectively. Furthermore, we investigated the electrical characteristics of the high-k Lu_2O_3 MOHOS-type memory devices.

2. Experimental

The integration of MOHOS-type memory device using a Lu_2O_3 charge trapping layer was started with 4-in p-type (100) substrates. After a traditional Radio Corporation of America (RCA) cleaning process, a 3-nm tunneling oxide was thermally grown at 950 °C by a vertical furnace. A ~6 nm Lu_2O_3 film was deposited on the tunneling oxide as a charge trapping layer by reactive sputtering from a lutetium target in diluted O_2 (Ar/O_2 = 5 sccm/2 sccm) at substrate temperature of 27 °C. The base pressure in the sputtering system was about 1×10^{-6} Torr and the growth rate of the film

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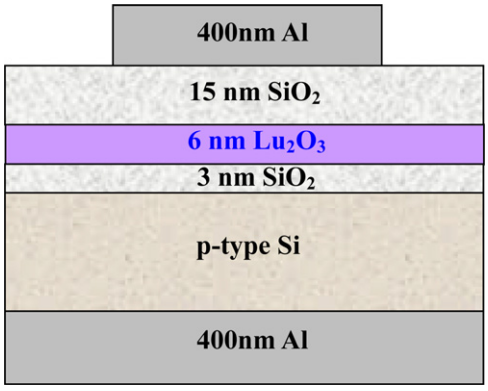

Fig. 1. Schematic representation of the Lu_2O_3 MOHOS-type memory device structure.

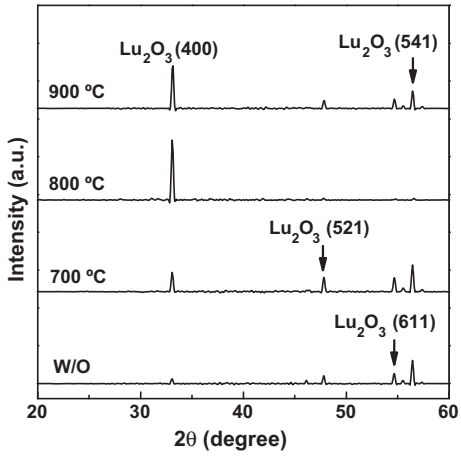

Fig. 2. XRD patterns of Lu_2O_3 films after RTA at different temperatures.

was 0.6 Å s^{-1}. During deposition the total pressure was maintained at ~10^{-3} Torr. Then, the samples were subjected to rapid thermal annealing (RTA) treatment by an incandescent lamp RTA method at various temperatures under an O_2 ambient for 30 s. A 15-nm-thick (SiO_2) blocking oxide was deposited on the lutetia through plasma-enhanced chemical vapor deposition using tetraethoxysilane as the precursor at a substrate temperature of 300 °C. Subsequently, a 400 nm Al film was deposited on the blocking oxide as the gate electrode through thermal evaporation. The area of the MOHOS device was defined through wet etching. Finally, a 400-nm-thick Al film was deposited on the backside contact of the Si wafer. Fig. 1 illustrates the structure of the fabricated Lu_2O_3 MOHOS-type memory device.

The thicknesses of the tunnel oxide, blocking oxide and the storage layer were determined by spectroscopic ellipsometer. The film structure and composition of the lutetia films were examined using XRD and XPS, respectively. XRD analyses were performed using the grazing incidence of Cu K_α (λ = 1.542 Å) radiation. The bonding structures of the films were analyzed using a monochromatic Al K_α (1486.7 eV) source. High frequency capacitance–voltage (C–V) measurements were recorded at 0.1 MHz using an Agilent 4285A LCR meter. The dielectric constants of the films (before and after RTA treatment) were determined from the capacitances measured in the accumulation regions of the C–V curves.

3. Results and discussion

To study of the crystalline structures of the lutetia films, XRD measurements were performed on these films with and without RTA treatments. For the as-deposited film (W/O), one (5 4 1) and three relatively small (4 0 0), (5 2 1), and (6 1 1) peaks are found (REF: PDF 076-0162 and 012-0728), which means that the film is a polycrystalline structure as shown in Fig. 2. The temperature-induced of the crystalline structure of lutetia film can be followed by XRD analysis. With increasing PDA temperature up to 800 °C, only a strong (4 0 0) peak intensity was observed in the XRD patterns, possibly suggesting that the film is condensed during this annealing temperature to form a stoichiometric Lu_2O_3 film. One strong (4 0 0) and three weak (5 2 1), (6 1 1), and (5 4 1) diffraction peaks were present for the sample annealed 900 °C. Moreover, The intensity of the (4 0 0) peak of the film annealed at 900 °C was smaller than that of the film annealed at 800 °C, suggesting the formation of a silicate layer at the lutetia–oxide interface.

Fig. 3 shows the Lu 4d and O 1s peaks from the as-deposited and annealed film. Each fitting peak is assumed to follow the general shape of the Lorentzian-Gaussian function. Fig. 3(a) shows the Lu 4d XPS spectra of the Lu_2O_3/SiO_2 interface with and without RTA treatment. The Lu $4d_{3/2}$ and $4d_{5/2}$ double peaks of the Lu_2O_3 reference

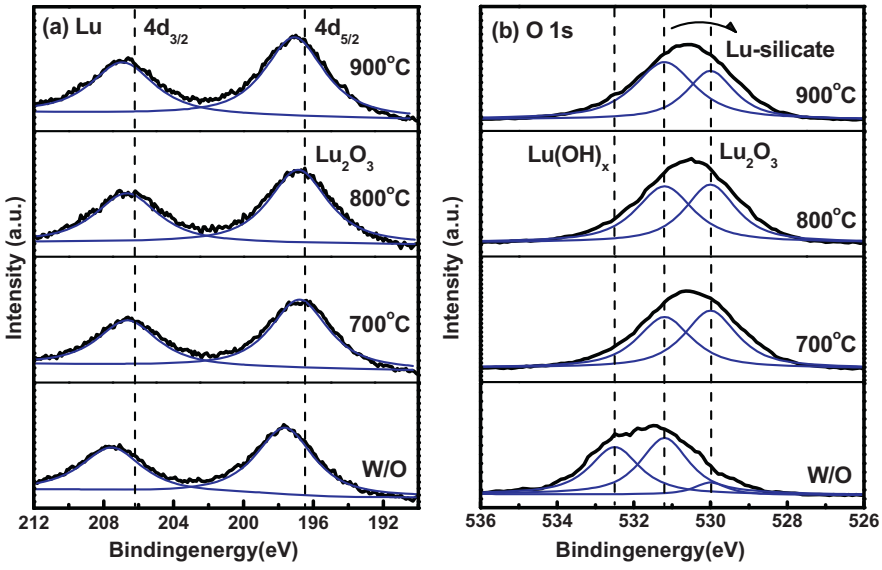

Fig. 3. XPS results of (a) Lu 4d and (b) O 1s in Lu_2O_3 films before and after RTA at different temperatures.