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# Current redistribution by intermetallic compounds in Through-Silicon-Via (TSV)

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ABSTRACT

Bi-metallic thin film redistribution layers, deposited in the Through-Silicon-Via (TSV), were stressed by electrical current for failure analysis. A new mechanism suggested that the formation of intermetallic compounds, at the corners of the vias, redistributed and reduced the electrical current at the current crowding region. This study proposes a model and deduces a kinetic analysis to demonstrate the effect of the current distribution caused by the volume of the compound. A simulation was used to substantiate the experimental and analytical results.



## 1. Introduction

This study introduces three-dimensional integrated circuit (3D IC) packaging since the trend with electronic devices is to enhance the performance while shrinking the dimensions. A key factor in 3D IC technology is Through-Silicon-Via (TSV) [1–7]. TSVs connect the signals between the chips and the bumps by using metallic thin film redistribution layers (RDLs). The electrical signals require conducting from the circuitry on one side of the chips to the solder bumps on the other through the vias. The high aspect ratio of the vias is the current manufacturing barrier that requires surmounting, by filling the electroplated Cu into the through-holes. However, the concept of TSVs has been widely adopted in Complementary Metal-Oxide-Semiconductor (CMOS) image sensors that do not necessitate high-density circuitry; hence, the dimension of the vias can be enlarged [8,9]. To reduce the cost of the manufacturing process, depositing metallic thin films that cover the free surfaces of the vias without completely filling it could serve as RDLs in the sensor devices.

In this study, the RDLs are Al(4 wt.% Cu)/Ni bi-layer thin film. The electromigration in Al(Cu) lines has been studied extensively [10–14]. The Cu in the Al lines could retard the electromigration effect when the $Al_2Cu$ intermetallic compound (IMC) is formed, and preferentially precipitates in the grain boundaries of Al. The dissolution of the precipitates results in a reduction or reversal of the flux of Al, to reduce the failure of Al lines. Furthermore, the Ni layers were deposited on top the surface of the Al(Cu) traces to secure the conducting paths. The dimensions of the Al(Cu) traces were larger than those in the IC and did not possess the bamboo structure. However, the length of the conducting lines was significantly longer than that required for the back stress to effectively prohibit the deformation. The RDLs in the vias were exposed to the air without the dielectric layer, which might induce early failure. The characteristic 3D vias yielded a complicated configuration, with many turns and corners, that would result in the divergence of electrical flux. By using a sputtering technique, the Al(Cu) traces deposited on the sidewall were thin (only several hundred nanometers); therefore, the current crowding at the corners of the vias would reduce the lifespan considerably.

This paper discusses the redistribution phenomenon of the electric current due to the formation of $Al_2Cu$. A model is proposed to describe and verify the experimental results. The concept could be applied to the general behaviors of vertical conducting paths in a 3D structure. A possible architecture in 3D-stacked IC devices is to conduct the electrical current from Cu vias to the Sn-based solder microbumps through Cu RDLs. The intermetallic compound formation between Cu and Sn would be spontaneous at room temperature, and become prominent through current stressing. The effect on current flow caused by the formation of these phases should not be disregarded. This study provides a kinetic analysis and simulation results to interpret the experimental results and fortify the physical concept of current redistribution.

## 2. Experimental

The Through-Silicon-Via (TSV) test samples were provided by Xintec Inc. The Si wafer was thinned down to approximately 150 μm by using chemical–mechanical polishing. On the rear of

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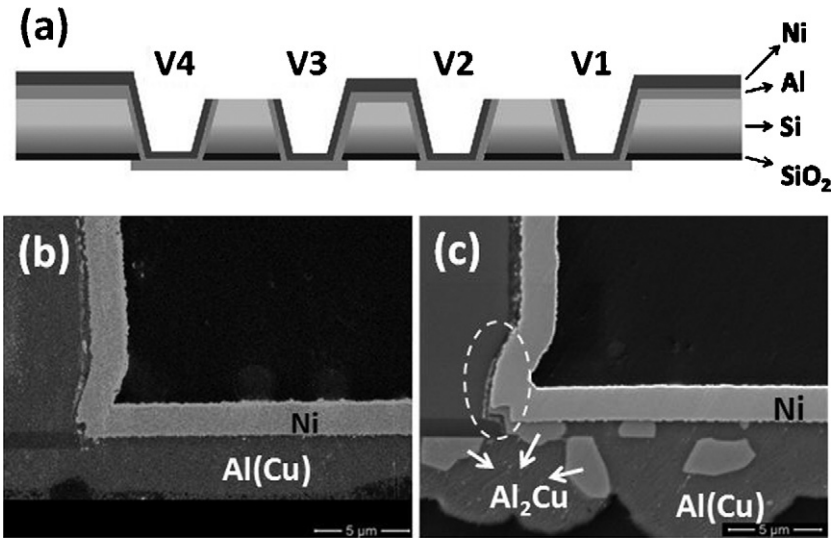


**Fig. 1.** (a) The schematic drawing of the test vehicle with Through-Silicon-Vias. The vias are labeled V1–V4 from right to left. (b) Enlarged SEM images of the bottom left corner of via before current stressing. (c) Enlarged SEM images of the bottom left corner of via, V2 after current stressing at $5 \times 10^5$ A cm$^{-2}$ at 200 °C for 50 h.

the Si wafer, a 1-μm-thick $SiO_2$ layer was deposited as an insulator. Furthermore, a 3-μm-thick Al(Cu) layer was deposited by sputtering to enhance the mechanical strength of the samples. Four vias were present on each sample. These vias were etched by drying etching methods, and the etching was stopped when Al(Cu) layers were revealed. The vias were electrically connected by a series of Al(Cu)/Ni lines. The sputtered Al(Cu) lines were 96 wt.% Al and 4 wt.% Cu, with the dimensions of 1 μm ($h$) × 100 μm ($W$). Ni layers with a thickness of 3 μm were electroless plated on the Al(Cu) lines.

The samples were current stressed with a current density of $5 \times 10^5$ A cm$^{-2}$ at 100 °C and 200 °C for 50 h. A set of 6 samples was current stressed. After applying the current, 2 samples failed within a short time. This failure could be attributed to the floating fabrication parameters of the test vehicles. Without immediate failure, 4 samples survived under current until the resistance met the criteria of failure. The samples were embedded in epoxy and cross-sectioned after current stressing. The cross-sectional images were examined by scanning electron microscopy (FE-SEM, HITACHI S-4700). A 2D matrix of pixels was used to simulate the current distribution in the conducting lines. The algorithm of the simulation can be referred in Ref. [15].

## 3. Results and discussion

Fig. 1(a) is a schematic drawing of the vias and the conducting lines. These vias were labeled V1, V2, V3, and V4, from right to left. The electric current flew along the Al(Cu)/Ni layers, and is indicated by the arrow symbol. The undercut of the vias at the lower corners was inevitable due to the manufacturing processes, and could cause sharp turns of the Al(Cu) and Ni traces. Fig. 1(b) and (c) shows the cross-sectional images of the lower left corner of V2 before and after stressing, respectively, under the current density of $5 \times 10^5$ A cm$^{-2}$ at 200 °C for 50 h. In one via, the bottom left corner could be regarded as the anode, while the bottom right was the cathode. Many $Al_2Cu$ compounds precipitated in the conduction of the Al(Cu) trace after current stressing. The irregular shape at the bottom of the sample was the hillocks, which were caused by electromigration. These Al(Cu) traces in the dotted circled region were depleted under the current since they were at the cathode ends of the sidewalls. In Fig. 1(c), the $Al_2Cu$ compounds not only precipitated at the bottom of the vias, but also grew in the direction against the electric current flow direction, and formed a continuous layer at the undercut area. Fig. 2 shows the reduced resistance measurement of the 4 conducting lines versus current stressing time. By assuming a 20% increase of the resistance as the failure criteria, these samples would not fail for over a day. Some samples could survive for over a week. The inserted figures represent the corresponding cross-sectional images of 1, 4, and 8 h of current stressing. The reduced resistance displayed a drastic variation in the first several hours, and became stable afterward. The $Al_2Cu$ layer gradually increased with current stressing time. After 8 h, the compound filled the gap between Ni and the $SiO_2$ insulating layer. The steady increase of resistance could be regarded as the dissolution of Ni in the Al traces. It could also possible that the increasing volume of $Al_2Cu$ raised the resistance. The early failure was seemingly avoided, and the current detoured to the Ni layers. The detour reduced the current density in the thin Al(Cu) traces on the sidewall, and maintained a conducting path for current. In Fig. 1(c), the Al(Cu) traces at the corner shrunk from 4 μm to 1 μm, and are the divergence points where current crowding appeared. When the current spread to the Ni lines, current crowding was still expected to raise the local current density, enhance Joule heating, and result

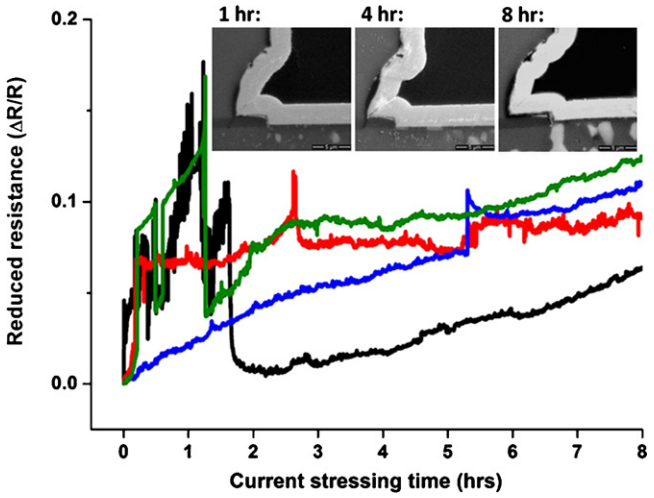


**Fig. 2.** The reduced resistance of the samples versus the current stressing time. The inserted figures correspond to current stressing of 1, 4 and 8 h.