Available online at www.sciencedirect.com
ScienceDirect
Materials Chemistry and Physics 104 (2007) 350–355
MATERIALS CHEMISTRY AND PHYSICS
www.elsevier.com/locate/matchemphys

Thermally induced interfacial interactions between various metal substrates and a-SiC thin films deposited by a polymer-source chemical vapor deposition

Y. Awad [a,b,*], M.A. El Khakani [c], C. Aktik [a], J. Mouine [a], N. Camiré [b], M. Lessard [b], M. Scarlete [d]

[a] *Université de Sherbrooke, Sherbrooke, Québec, Canada J1K 2R1*
[b] *SiXtron Advanced Materials Inc., Sherbrooke, Québec, Canada J1J 2E8*
[c] *Institut National de la Recherche Scientifique, INRS-ÉMT, Varennes, Québec, Canada J3X 1S2*
[d] *Bishop's University, Lennoxville, Québec, Canada J1M 1Z7*

Received 12 March 2007; accepted 20 March 2007

Abstract

Amorphous silicon carbide (a-SiC) thin films have been deposited onto a variety of substrates, including silicon, SiO_2, Si_3N_4, Cr, Ti and refractory metal-coated silicon, by means of a polymer-source chemical vapor deposition (PS-CVD), at a substrate temperature of 800 °C. The poly(dimethylsilane) (PDMS) was used as a high-density single-source molecular precursor for the PS-CVD process. Capacitance–voltage (*C–V*) measurements were systematically used to evaluate the impurity level of the deposited a-SiC films. In addition, elastic recoil detection (ERD) and X-ray photoelectron spectroscopy (XPS) techniques were used to determine the elemental composition of the films and their interface with substrates. Scanning electron and atomic force microscopies were also employed to characterize the surface morphology of the films. The impurity levels of the a-SiC films were found to be clearly correlated with the nature of the underlying substrates. The Pt–Rh and TiN-coated Si substrates are shown to lead to the lowest impurity level ($\sim 1 \times 10^{13}$ cm^{-3}) in the PS-CVD grown a-SiC films, while Cr and Ti-coated Si substrates induce much higher impurity concentrations. Such high impurity levels are shown to be a consequence of a strong metallic diffusion of the metallic species (Cr or Ti). In contrast, no diffusion was observed at the interface of a-SiC with either Pt–Rh or TiN. Our results pinpoint TiN-coated Si as the electrode material of choice that satisfies best all the criteria required for the integration of a-SiC into opto-electronic devices.

Keywords: Interfaces; Carbides; Polymers; Semiconductors

1. Introduction

Amorphous silicon carbide (a-SiC) thin films continue to attract considerable attention because they are highly promising for a variety of applications spanning from passive coatings for very harsh environments to active opto-electronic devices. The wide range of applications of a-SiC is due to their unique combination of excellent properties, such as the wide bandgap [1], high breakdown electric field [2], unprecedented mechanical properties [3] and chemical inertness (due to the covalent Si–C bonding energies). Indeed, a-SiC films have been extensively investigated for applications such as optoelectronics devices [4], solar cells [5], phototransistors [6], light emitting diodes [7], color sensors [8], photomodulator devices [9] and flat-screen full color displays [10]. In a large part of these applications, the a-SiC films have to be contacted with metal electrodes. As a consequence, the control of the quality of the a-SiC–metal interface is a crucial issue that should be addressed as a function of the targeted application. Indeed, while the interdiffusion between metal and SiC can be considered advantageous in some applications (for example, joint between a-SiC and Ni-based super alloys [11,12] it is however non-desired in many a-SiC based devices intended for high temperature and high power applications. In fact, under high temperature conditions, the metallization contacts of a-SiC degrade severely because of many factors such as the interdiffusion between layers, compositional and structural changes, thermal and/or structural induced stress that can take place at the

* Corresponding author at: Université de Sherbrooke, Sherbrooke, Québec, Canada J1K 2R1. Tel.: +1 514 2503235; fax: +1 450 6528634.
E-mail address: yawad@sixtron.com (Y. Awad).

0254-0584/$ – see front matter © 2007 Elsevier B.V. All rights reserved.
doi:10.1016/j.matchemphys.2007.03.030

metal/semiconductor interface. Silver has been even reported to evaporate from the SiC surface at temperatures above 600 °C [13]. A fair number of studies have been reported on the interface reactions between SiC and metals (including Ti [14], Cr [15], Ta [16], Mo [17], Ni–Cr alloy or TiAl [18]). These reports have shown that the reaction product sequence and interface morphology in SiC/metal reactions are mainly dependent on the contact materials. For example, in the case of SiC and Ni [19], Co [20] or Pd [19] the formation of less metal-rich silicides usually occurs and a periodic morphology composed of alternating carbon and silicide has been evidenced [21]. Other metals such as Ti [22], Mo [23], Fe [24], Nb [25] and W [26] formed both carbides and silicides after annealing at temperatures between 570 and 1200 °C, the product phases in Ti/SiC were reported to be TiC [27] and $TiSi_3$ [28]. Thus the reactions of a-SiC with many metals at potential device operating temperatures of ∼600 °C severely limit the use of a-SiC-based device. Therefore, it is important to develop contacts which are stable at high temperatures. Alternatively, one may consider the use of diffusion barriers to prevent the interdiffusion at the metal–SiC interface. In fact, different alloys [28] including Al_2O_3, TiB_x, VB_x and TaB_x were tested as a diffusion barrier between Ti and SiC, but none of them was found to stop effectively the diffusion of Ti into the SiC layer at a temperature of 900 °C. Finally, it is to be emphasized that most of the work related to SiC/metal interface that has been covered in literature is based on depositing metal films on SiC substrates, but very few started with metal as a substrate.

In this paper, we report on the deposition of a-SiC thin films by means of a novel PS-CVD process onto various metallized substrates. The focus is put here on the study of the interfacial interactions between a-SiC and the various underlying metals with the aim to identify the most chemically stable metal electrodes for the integration of a-SiC into various opto-electronic devices.

2. Experimental

Amorphous SiC thin films were deposited from poly(dimethylsilane) (PDMS) using an in-house built reactor. Details of the furnace and deposition conditions were reported elsewhere [29,30]. The reactor used in this study was a Lindberg single-zone programmable tube furnace equipped with a Eurotherm PID temperature controller working up to 1100 °C and providing an accuracy of ±1 °C at 1000 °C. The tube in the furnace is usually 50 in. in length and from 3 in. in diameter. The tube is surrounded by heating elements which also incorporate a thermocouple. The rate of heating was 8 °C min^{-1}. Prior to the deposition, the chamber was pumped to a background pressure of 2.5×10^{-2} Torr. Ultra high purity (UHP) argon (99.999%) gas was then introduced into the chamber. This process of pumping and reintroducing the UHP argon was repeated four times to ensure that no oxygen remained in the chamber. The substrates and the solid polymer-source were introduced in the quartz tube from the opposite ends of the reactor through load lock systems. Samples were placed inside the tube in ceramic boat using a long push rod. The PDMS source was put in a ceramic boat and pushed inside the furnace where the temperature is 350 °C at which the sublimation process started. Ar was then introduced to carry the sublimated gas through the furnace to pass over the substrates. The deposition time was fixed at 15 min at 800 °C, and the samples were systematically left in the chamber for an incubation period of 2 h at 800 °C before getting them out of the furnace. This incubation time was chosen to investigate the relative stability of the interface between the metallized substrates and the PS-CVD deposited a-SiC films. The metallized substrates were prepared by depositing various metallic thin films on Si wafers. These metallic thin films include refractory metals (Cr, Ti and V), high oxidation resistant metals and alloys (Ni, Ni–Cr, Au and AuPd). Furthermore, two alloys (TiN and Pt–Rh) were also used as substrates for their known excellent oxidation resistance. The thickness of all a-SiC films deposited on various substrates was 150 nm, except the case of TiN thin metallic films on which the a-SiC thin films were 200 nm as determined by cross-sectional view of SEM. In addition, Si substrates coated with 1 μm thick thermally grown SiO_2 and LPCVD Si_3N_4 were also used in this study. The impurity level in the a-SiC films was evaluated using capacitance–voltage technique (*C–V*). The *C–V* measurements are carried out using mercury probe technique. The dc bias voltage is varied from −10 to 10 V. Increasing the voltage will result in an increase in the width of the depletion zone (X_d) which will alter the capacitance of *C* as given in the following equation

$$X_d = \frac{A\varepsilon_s}{C} \tag{1}$$

where X_d is the depth from the surface, *C* the measured capacitance, *A* the capacitor area and ε_s is the semiconductor permittivity. By measuring the capacitance, *C*, of a semiconductor capacitor at applied bias, V_A, the doping $N_d(X_d)$ is obtained as a function of position, *X*, by the following equations [31]

$$N_d(X_d) = \frac{-C^3}{q\varepsilon_s(dC/dV)} \tag{2}$$

where N_d is the doping (impurity) concentration and *q* is the electron.

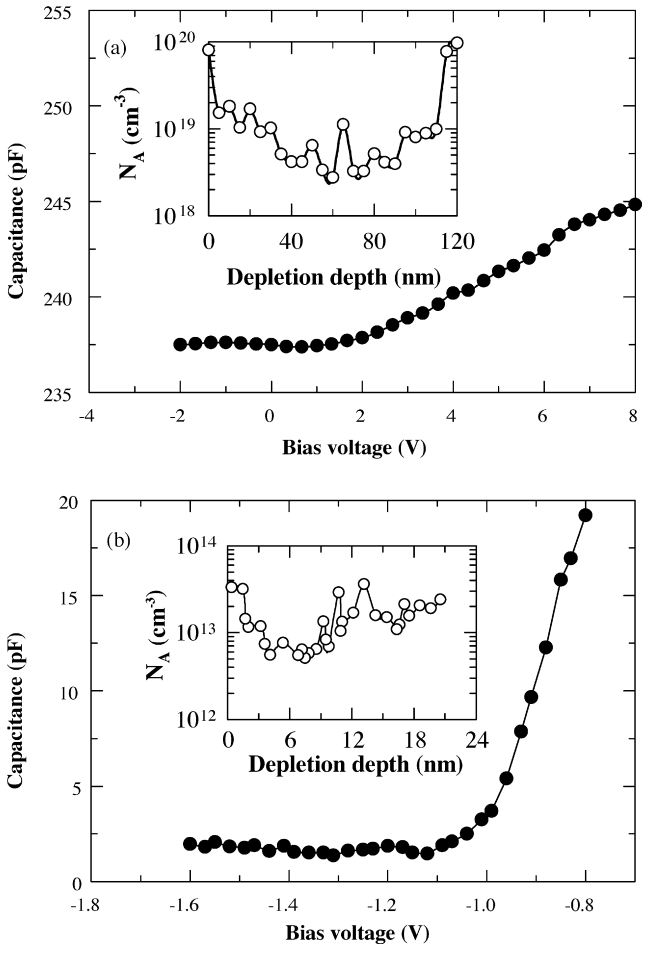

Fig. 1. Variation of high frequency capacitance with respect to bias voltage measured using mercury probe technique for a-SiC thin films deposited on: (a) Cr-coated Si (set I) and (b) Pt–Rh-coated Si (from set III). The inset represents the carrier concentration with respect to depletion depth extracted from the corresponding *C–V* characteristic curves.