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Improvements to the solar cell efficiency and production yields of low-lifetime wafers with effective phosphorus gettering

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ABSTRACT

This research focuses on the improvement of solar cell efficiencies in low-lifetime wafers by implementing an appropriate gettering method of the diffusion process. The study also considers a reduction in the value of the reverse current at −12 V, an important electrical parameter related to the hot-spot heating of solar cells and modules, to improve the product's quality during commercial mass production. A practical solar cell production case study is examined to illustrate the use of the proposed method. The results of this case study indicate that variable-temperature gettering significantly improves solar cell efficiencies by 0.14% compared to constant-temperature methods when the wafer quality is poor. Moreover, this study finds that variable-temperature gettering raises production yields of low quality wafers by more than 30% by restraining the measurement value of the reverse current at −12 V during solar cell manufacturing.

1. Introduction

The photovoltaic industry has been undergoing rapid growth, with worldwide production of photovoltaic modules exceeding 20 GW in 2011 [1]. The key components driving the economic viability of solar power have been high-efficiency modules, highly productive manufacturing lines and low material costs. The majority of photovoltaic modules are now produced from multicrystalline silicon (mc-Si) solar cells. Therefore, low-cost wafers and high production volumes make mc-Si a promising material for use in low-cost, high-efficiency, and high-quality solar cells to fulfill the requirements for high efficiencies and product quality in solar modules [2]. However, mc-Si can contain high impurity concentrations and defects that affect the minor carrier's lifetime and limit the solar cell's performance [3]. In addition, a solar wafer contains large quantities of impurities and contaminant residues that can induce electrical failure and hot-spot heating [4].

Over the past two decades, research has focused on identifying impurity gettering methods for mc-Si solar cells, including boron gettering [5], aluminum gettering [6], and phosphorus gettering [7,8,9]. Phosphorus gettering (p-gettering) is known to enhance the removal of impurities, resulting in an increase in the minority carrier lifetime of solar-grade silicon. In addition, p-gettering does not add an extra step to the existing solar cell production process [10,11], a key requirement identified by previous researchers [12–16].

However, an extended single high-temperature gettering step suffers from thermal degradation, and has therefore been deemed unsuitable for improving gettering results [17]. A long gettering process time also leads to high residual impurity concentrations and is unsuitable for commercial mass production [8]. Plekhanov et al. [6] have proposed a numerical model of a variable-temperature gettering process using low-temperature gettering tails to shorten the required gettering time and achieve low residual impurity concentrations. Since the introduction of this variable-temperature gettering method, its strengths have been described extensively in the literature for applications that improve minor carrier lifetimes [18,19] and shorten the duration of the diffusion step, as required for commercial production [8]. This method has proven effective at reducing unwanted impurities, and has been introduced as a functional method to aid researchers in increasing the conversion efficiency of solar cells based on lifetime predictions [5]. Some researchers have evaluated this gettering effect using small samples [20].

Despite the large number of studies that have implemented variable-temperature p-gettering to improve the lifetimes of solar cells hindered by low-lifetime wafers, a practical solution for its commercial application has not yet been identified. Most research to date has incorporated only a few samples to illustrate the connection between wafer minor carrier lifetimes and mc-Si solar cell efficiency [2,19]. However, the quality of the mc-Si material is not a constant, but varies among suppliers and even from ingot to ingot when obtained from the same supplier [21]. Therefore, one cannot generalize the results obtained from a few samples to accurately describe all mc-Si material used in the processing of solar cells. From the literature review, it is apparent that there is limited

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research focusing on how to improve solar cell efficiency and quality in commercial solar cell production with p-gettering. The data in this study are gathered through mass-production data measurements and are therefore highly reliable.

The present study analyzes the strength of a variable-temperature p-gettering process, using wafers of differing quality, at improving solar cell efficiencies and production quality. Section 2 discusses the experimental details of a quantitative comparison of the enhanced solar cell efficiencies of wafers with varying quality, while Section 3 presents the experimental results and implications of the experimental analysis. The conclusion and future research directions are described in Section 4.

2. Experiment

This experiment is performed with p-type 180-μm-thick mc-Si wafers with an area of $12.6 \times 12.6\,cm^2$ and a resistivity of 0.5–3 Ωcm. It should be mentioned that before going forward to manufacture the solar cell, neither the removal of native oxide layer nor any cleaning procedure was applied.

2.1. Case study

The manufacturing at Gintech Energy Corporation, a solar cell manufacturing company in Taiwan, is investigated in this case study. The principal mass-production processing steps at this company and in the case study are shown in Fig. 1 and described below.

(1) Surface texturing: After sorting, the silicon wafer saw marks are eliminated and the wafer surfaces are rough-etched using acid. This processing step is normally used to create a textured surface that will reduce the total reflection of incident light and increase the wafer's efficiency.
(2) Phosphorus diffusion: Phosphorus gas is injected into the wafer in a high-temperature chamber to create electrical holes in the rich p-type silicon wafer's surface, which are then infiltrated with phosphorus to form an n-type area containing a greater quantity of electrons. This process is the so-called formation of a P–N junction for photovoltaic conversion effects. The phosphorous diffusion is performed in a quartz tube furnace using $POCl_3$ and O_2. During the high temperature diffusion process, $POCl_3$ could be decomposed to PCl_5 which is highly corrosive and cause damage to the wafer surface. Therefore, O_2 is induced to react with PCl_5 to form P_2O_5 and reduce the PCl_5 as much as possible. The typical thickness of oxidation layer and phosphorous gettering layer is about 30 and 200 nm, respectively; both of these layers were removed by hydrofluoric acid (HF) after.
(3) Phosphorus glass etching: During the phosphorus diffusion process, silica-phosphate glasses on the outer surface of the wafers are created. The silica-phosphate glasses must be removed with HF washing to continue follow-up solar cell process.
(4) Plasma-enhanced chemical vapor deposition (PECVD): The interaction of silane and ammonia in the vacuum furnace of a PECVD system can create a thin silicon nitride SiN_x:H layer that serves as an antireflection coating. In addition to its optical benefits, this dielectric coating can improve the electrical properties of the cell by surface passivation. The deposition occurs at temperatures of approximately 400 °C.
(5) Screen printing: A conductive paste of silver and aluminum is used to screen print thin and thick electrodes onto both surfaces of the wafer. This process includes three steps: printing of the front sides, printing of the thick electrode, and using the aluminum paste to print the remaining area on the reverse side. Between each printing step, the wafer must pass through the drying furnace (200 °C for 9 min) and optical testing system to confirm that the screen printing details and positioning are correct.
(6) Rapid sintering: Once the metal paste has gone through the screen printing and drying steps, it is rapidly sintered to penetrate the silicon nitride coating on its front and infiltrate the wafer's surface binding tightly to conduct the electrical current. A full aluminum layer printed on the back of the cell, with subsequent alloying via firing, in a belt furnace with a set peak temperature of 920 °C and a belt velocity of 6 m/min, produces a back-surface field (BSF) and improves the cell bulk.
(7) Edge isolation: The front side of a solar cell made from a p-type silicon wafer is negative (−) and the back is positive (+). A notch, deeper than the P–N junction on the wafer's edge, is cut using laser dicing to avoid a short circuit between the positive and negative sides. This process can also be performed during the plasma treatment and chemical etching stages.
(8) Performance testing and classification: Once the appearances of the wafer's front and back surfaces are examined, its photovoltaic conversion efficiency and other electrical characteristics are measured using automatic testing equipment. The samples used for cell analysis are measured in the solar simulator under $100\,mW/cm^2$ (AM 1.5) illumination, and the electrical performance and conversion efficiency of the solar cell are simulated by measuring the power output under a Berger flash system with AAA-class spectrum, uniformity, and temporal stability. After performance testing, the cell sorter typically classifies the products based on cosmetic and electrical parameters and sorts them into different product grades and cell stacks.

2.2. Experimental scheme

The proposed experimental scheme in this study is shown in Fig. 2.

2.2.1. Wafer sorting according to lifetime characteristics

Prior to processing, the wafers are sorted using a wafer inspection system (WIS), which separates wafers with varying lifetime specifications using a micro-photoconductivity decay (μ-PCD) method. The wafer sorting process typically classifies the incoming wafers based on parameters such as material lifetime, resistivity, microcracks, and others, and sorts them into different cell stacks.

The mc-Si wafers used in this study are provided by two different suppliers, S_A and S_B. Wafers from the first supplier, S_A, are made from high-quality ingot and their base minority carrier lifetimes are greater than 1.4 μs. Parts of the wafers from the second supplier, S_B, do not meet the cell manufacturer's quality specifications, which require minority carrier lifetimes of at least 0.8 μs. The results of the mass production of the wafers provided by suppliers S_A and S_B are shown in Table 1.

Table 1 defines five product categories. A-grade solar cells are prime flawless solar cells, while B-grade cells are solar cells containing visual flaws that do not affect the power. C-grade solar cells are those with flaws that affect the power output, so the output conversion efficiency is less than 12.5% for whatever reason. R-grade solar cells are those with flaws that affect the measured R_{sh} values, so the output R_{sh} is lower than 10 Ω for whatever reason, while I-grade solar cells are those with flaws that affect the measured reverse current at −12 V ($Irev_2$), so the output $Irev_2$ is greater than 2.5 A. The production yield is equal to the ratio of A-grade cells to other cells. The other product grades are generally considered scrap.

As shown in Table 1, the solar cells mass produced from the S_B wafers exhibit lower efficiencies than the cells produced from S_A wafers, with results typically approximately 0.33% lower. Moreover, the ratio of A-grade products from the S_A wafers is significantly higher than that from the S_B wafers due to failure of the