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# Eutectic and solid-state wafer bonding of silicon with gold

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ABSTRACT

The simple Au—Si eutectic, which melts at 363 °C, can be used to bond Si wafers. However, faceted craters can form at the Au/Si interface as a result of anisotropic and non-uniform reaction between Au and crystalline silicon (c-Si). These craters may adversely affect active devices on the wafers. Two possible solutions to this problem were investigated in this study. One solution was to use an amorphous silicon layer (a-Si) that was deposited on the c-Si substrate to bond with the Au. The other solution was to use solid-state bonding instead of eutectic bonding, and the wafers were bonded at a temperature (350 °C) below the Au—Si eutectic temperature. The results showed that the a-Si layer prevented the formation of craters and solid-state bonding not only required a lower bonding temperature than eutectic bonding, but also prevented spill out of the solder resulting in strong bonds with high shear strength in comparison with eutectic bonding. Using amorphous silicon, the maximum shear strength for the solid-state Au—Si bond reached 15.2 MPa, whereas for the eutectic Au—Si bond it was 13.2 MPa.



## 1. Introduction

Wafer bonding has been widely used as a key step in the integration of micro-electro-mechanical systems (MEMS). Several techniques have been developed for wafer bonding, such as silicon fusion bonding [1,2], anodic bonding [3], solder bonding [4], adhesive bonding [5], thermocompression bonding [6] and eutectic bonding [7]. Compared with other bonding methods, eutectic bonding has benefits such as large fabrication yield, high bond strength, good reliability and low resultant stress in the final assembly, as a result of the low process temperature [8]. Various eutectic systems have been reported and studied, such as Au—Sn, Au—Si, Al—Ge, Au—Ge and Au—In. The main advantages of the Au—Si system are its compatibility with Al interconnects due to the low process temperature [9], good mechanical stability and the absence of intermetallics which can cause fabrication issues. Au—Si is used in microfabrication because of its high bonding strength, excellent hermeticity which permits vacuum wafer-level packaging and good tolerance to surface topography as a result of the formation of a liquid phase [10,11]. It is also a good heat sink for packaged devices such as high power transistors, lasers and LED devices [12]. Au—Si eutectic bonding is not without its limitations; however, including high cost (due to the presence of Au), high modulus of elasticity, limited die size and the potential for chip damage [13].

As shown in Fig. 1 [14], the melting point of the Au—Si eutectic alloy is around 363 °C while the melting points of Au and Si are 1064 °C and 1414 °C, respectively. The eutectic composition is 19 at% (3 wt%) Si and 81 at% (97 wt%) Au. The solid solubilities of Au and Si in each other are very limited. During eutectic bonding, as the temperature is increased, diffusion of Au and Si occurs. When the composition reaches the eutectic composition, the liquid phase will form which accelerates the diffusion process [8].

Research has been done on various aspects of Au—Si bonding. Chen et al. introduced amorphous Si (a-Si) as a substitute for crystalline Si (c-Si) in Au—Si eutectic bonding [15]. They showed that an a-Si layer on a (1 0 0) Si wafer rapidly reacts with the Au layer and forms a uniform Au(Si) liquid alloy, which prevents the formation of air voids at the bond interface. Lin et al. studied the development of and evaluated Au—Si eutectic wafer bonding [16]. In their work, material composition, adhesion layer, electrical insulation, bonding parameters and surface pre-treatments were discussed in terms of bond performance. Lani et al. worked on several Au metallization schemes for Si wafers that were eutectic bonded [17]. They found that Au/Pt/Ti and Au/Ti/$SiO_2$ had the best characteristics for wafer bonding, while Au/Ni/Ti was not suitable for eutectic bonding. It was also demonstrated that surface roughness and resistance are good indicators of interdiffusion phenomena. Jing et al. investigated and compared two types of Au–Si wafer bonding structures (i.e., Au/Si and Au/Au) [9]. They suggested that non-uniformity of the Au/Si reaction is due to the native oxide on the bare Si surface, which results in poor bond quality for Au/Si bonds. In order to improve the bond quality, a Au/Au bonding structure was adopted and it was shown that the bond yield, bond repeatability and average shear strength was improved. Chen et al. [15] reported crater

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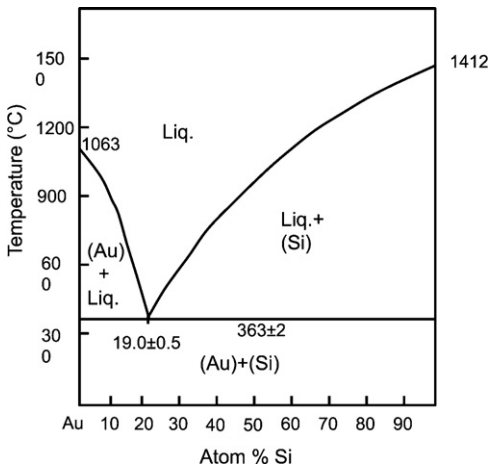


**Fig. 1.** Au—Si phase diagram [9].

formation at the interface when Au is bonded to crystalline Si (c-Si). This is a result of anisotropic Au and Si reaction. Silicon atoms located at higher energy crystal planes tend to dissolve into Au more easily. In c-Si, {1 1 1} planes have the lowest surface energy, so that the Si atoms on the {1 1 1} plane resist dissolution leading to the formation of V-shaped craters with {1 1 1} facets. One solution to the preferential dissolution and subsequent crater formation is to coat the c-Si wafer with an amorphous Si (a-Si) layer. This is also likely to shorten the bonding time. Amorphous Si does not have any preferential dissolution planes and has a lower density than c-Si, so that it should form a liquid Au—Si mixture more rapidly without crater formation [9].

The typically used Au—Si eutectic bonding temperature is 400 °C, but there are two issues with this condition. First, this temperature may be too high and can damage devices on the wafer during the bonding process [9]. Second, the formation of the liquid phase increases the risk of spill out of the Au—Si liquid, which can also damage the devices on the wafer [10]. In this work a solid-state wafer bonding process, which relies on solid-state diffusion, is proposed as an alternative to eutectic bonding. During solid-state diffusion bonding, temperatures lower than eutectic temperatures can be used (350 °C in this study), so the risk of thermal damage to devices is lowered and spill out of molten solder is prevented. This approach is similar to the thermocompression wafer bonding reported by Park et al., where they bond Au to Au instead of Au to Si in this work [6]. The potential advantage of the latter is that a composite bonded layer is formed, consisting of soft, ductile Au and hard, brittle Si, which in the proper proportions should improve mechanical properties. This work is divided into two components. Initially, solid-state diffusion experiments are undertaken, using Au/a-Si and Au/c-Si thin film diffusion couples. This is followed by bonding tests, comparing solid-state bonding with eutectic bonding, using both c-Si and a-Si. The primary focus is microstructural characterization, although limited correlation with mechanical testing is also done.

## 2. Experimental methods

In order to understand the diffusion mechanisms during solid-state Au—Si wafer bonding, annealing experiments were performed on Au/a-Si and Au/c-Si diffusion couples. The native oxide from ⟨1 0 0⟩ oriented Si wafers was removed by RF etching for 2 min at 250 V bias with a base pressure of 133 Pa. An a-Si layer (2 μm) was deposited immediately after cleaning by plasma enhanced chemical vapor deposition (PECVD) followed by sputtering of 800 nm of Au directly on a-Si. For the c-Si samples, after cleaning, a thin

**Table 1**
Deposition parameters for diffusion couple experiments.

| Sample | Layers | Thickness | Deposition parameters |
|---|---|---|---|
| Au/a-Si/c-Si | Au | 800 nm | Sputtered<br>1 kW in 133 Pa Ar<br>Deposition rate of 12 nm/min |
| | a-Si | 2 μm | PECVD<br>133 Pa base pressure<br>30 sccm $SiH_4$ and 500 sccm He |
| Au/Ti/c-Si | Au | 200 nm | Sputtered<br>1 kW in 133 Pa Ar<br>Deposition rate of 12 nm/min |
| | Ti | 10 nm | Sputtered<br>1 kW in 133 Pa Ar<br>Deposition rate of 12 nm/min |

Ti adhesion layer (10 nm) was deposited followed by deposition of the Au layer (200 nm). The layer thicknesses and deposition parameters are summarized in Table 1. The wafers were sectioned into 8 mm × 8 mm squares using a diamond saw. The samples were annealed at three different temperatures (250, 300 and 350 °C) in a tube furnace for 10, 20 and 30 min in forming gas (5% $H_2$–95% $N_2$) to minimize Si oxidation. After cooling, the samples were cleaved and cross sections of the fracture surfaces were examined by scanning electron microscopy (SEM) using a JEOL JAMP 9500F field emission Auger microprobe. The instrument was operated as an SEM using an accelerating voltage of 15 kV and a working distance of 22.4 mm; secondary electrons (SE) were used to form the images. Focused ion beam (FIB) methods were applied to prepare site specific transmission electron microscopy (TEM) samples for higher resolution examination. A Hitachi NB5000 dual beam FIB/SEM, operated at 30 kV, was used for this purpose with a 7 nm $Ga^+$ beam as the ion source. A JEOL 2010 TEM, operated at 200 kV and equipped with a Noran ultra-thin window (UTW) X-ray detector, was used for imaging and high spatial resolution diffraction and composition analysis.

Silicon wafers, ⟨1 0 0⟩ oriented and 100 mm in diameter, were used for bonding. The processing details are summarized in Table 2 and are briefly described below. The native oxide was removed by RF etching for 2 min at 250 V bias with a base pressure of 133 Pa. Immediately after removing the oxide, 100 nm of TiW was sputtered onto half of the wafers (the other half of the wafers was used to deposit a-Si) using a plasma enhanced sputtering system. The TiW acts as a diffusion barrier and an adhesion layer for subsequent Au deposition. Following this step, 800 nm of Au was sputtered under the same sputtering conditions as TiW. For a-Si wafer samples, after wafer cleaning, 800 nm of a-Si was deposited using low-pressure chemical vapor deposition (LPCVD). LPCVD was used because of its relatively low process temperature and low resultant stress in comparison with PECVD. For the entire a-Si layer to be consumed in forming the eutectic composition, the thickness of the Au layer would need to be about 3.9 times the thickness of Si

**Table 2**
Samples and deposition parameters for wafer bonding experiments.

| Sample | Wafer pairs | Thickness | Deposition parameters |
|---|---|---|---|
| a-Si | Au/TiW/c-Si | TiW: 100 nm<br>Au: 800 nm | Sputtered<br>1 kW in 133 Pa Ar<br>12 nm/min (TiW); 50 nm/min (Au) |
| | a-Si/c-Si | a-Si: 800 nm | LPCVD<br>550 °C and 40 Pa pressure<br>$SiH_4$ gas flow rate of 30 sccm for 6 h |
| c-Si | Au/TiW/c-Si | TiW: 100 nm<br>Au: 800 nm | Sputtered<br>1 kW in 133 Pa Ar<br>12 nm/min (TiW); 50 nm/min (Au) |
| | c-Si | – | – |