Short communication

Thermal conductivity of InAs quantum dot stacks using AlAs strain compensating layers on InP substrate

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ABSTRACT

The growth and thermal conductivity of InAs quantum dot (QD) stacks embedded in GaInAs matrix with AlAs compensating layers deposited on (1 1 3)B InP substrate are presented. The effect of the strain compensating AlAs layer is demonstrated through Atomic Force Microscopy (AFM) and X-ray diffraction structural analysis. The thermal conductivity (2.7 W/m K at 300 K) measured by the 3ω method reveals to be clearly reduced in comparison with a bulk InGaAs layer (5 W/m K). In addition, the thermal conductivity measurements of S doped InP substrates and the SiN insulating layer used in the 3ω method in the 20–200 °C range are also presented. An empirical law is proposed for the S doped InP substrate, which slightly differs from previously presented results.

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1. Introduction

The performance of thermoelectric materials depends on the figure-of-merit ZT, which is defined as $ZT = S^2\sigma T/\lambda$, where S is the Seebeck coefficient, σ the electrical conductivity, λ the thermal conductivity, and T is the absolute temperature. To obtain the highest figure of merit, the power factor defined as $S^2\sigma$ must be maximised and in the meantime the thermal conductivity must be minimised.

Several approaches have led to an enhancement of the figure of merit. Most of them have relied on the reduction of the thermal conductivity of conventional thermoelectric materials (e.g. BiTe/BiSbTe) by introducing various phonon scattering nanometre scaled defects including precipitates, grain boundaries, or superlattices. Epitaxial semiconductor nanostructures have been evidenced as very good candidates for obtaining a high figure of merit [1]. Bi_2Te_3/Sb_2Te_3 superlattices have been reported to have a ZT ∼ 2.4 at 300 K [2], while PbSeTe based quantum dots have reached a ZT up to 3 at 550 K [3]. Ge QDs on Si with 3 nm spacing layers have also shown a clear reduction in thermal conductivity (<1 W/m K) [4] which is a promising result for applications in thermoelectricity.

In the case of III–V compounds, InP and GaAs based quantum wells have first attracted some attention for monolithic thermal cooling of laser diodes [5]. If theoretical studies on the thermoelectric properties of III–V QDs have been proposed [6,7], very little thermal conductivity experimental data of such QDs are reported to our knowledge.

Recently, high quality ErAs nano-inclusions in AlGaInAs alloys grown on InP substrate have been proposed and successfully applied to thermoelectric applications. A ZT = 1.3 at 800 K has been demonstrated [8]. A route not yet explored is based on stacks of Stranski-Krastanov InAs nanostructures on InP substrate grown by molecular beam epitaxy (MBE). Owing to a relative small lattice mismatch (3.2%), different nanostructure morphologies have been evidenced in this system. On exactly oriented (1 0 0) surface, quantum dashes (QDashes) or quantum wires (QWires) elongated along the [1–10] direction nanostructures are easily obtained. The control and preservation of the morphology and the density from layer to layer when close stacking is however difficult [9].

On (1 1 3)B substrate however, well resolved QD facets are generally observed due to a higher buffer layer surface energy. This surface orientation is thus more favourable to control the stack of InAs QDs with reproducible morphologies from layer to layer. For instance, a stack of 150 InAs QD layers with 20 nm spacers grown by MBE has been realised [10].

Moreover, it is well known that strain accumulation during QD stack growth leads to surface degradation, or more severely, creation of defects, such as misfit dislocations. Dislocations are known

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to reduce the thermal conductivity [11] when present in rather high density, but are also responsible for a reduction of carrier mobility and sometimes also act as deep levels or conductive carrier channels. These dislocations are thus generally detrimental to thermoelectric performances of semiconductor materials.

Therefore, the stack of self assembled QDs generally requires a strain compensation technique.

We here show that by balancing the compressively strained Stranski-Krastanow InAs quantum dots using AlAs tensile strained layers, a high number of closely stacked quantum dot layers with good quality can be obtained.

In the following, the 3ω thermal conductivity measurement method is briefly presented and first applied to Si and InP substrate. The insulating Si_xN_y layer is also characterised in terms of thermal conductivity and interface thermal resistance. The growth of InAs QD stacks using AlAs as strain compensating layers is then presented. AFM imaging is used for structural analysis on two stacks of 20 QD layers, with and without insertion of the strain compensating layers. X-ray diffraction is used to analyse the structural quality of a stack of 100 QD layers and photoluminescence (PL) measurement is performed to reveal the optical quality of the layers.

The thermal conductivity of this stack is measured and shows a clear reduction when compared to a bulk lattice-matched GaInAs.

2. Thermal conductivity measurements using the 3ω method

2.1. Experimental details

The thermal conductivity measurements were performed using the so called "3ω method" developed by Cahill [12] with a modified model by Borca-Tasciuc to take into account the finite thickness of the substrate and adiabatic boundary conditions [13]. This method has proven to be well suited for epitaxial films. Basically, it consists in measuring the temperature rise in a metal line driven by an AC current, which simultaneously acts as a heater and a thermometer, as a function of the current frequency.

All samples were prepared using the same method. Typically, a 200 nm silicon nitride (Si_xN_y) insulating layer was deposited by PECVD (plasma enhanced chemical vapour deposition) at 250 °C. A Ti(20 nm)/Au(200 nm) was subsequently deposited by e-beam evaporation and lift-off processed, resulting into a 10 mm long and 20 μm wide heating metallic stripe with two 2 mm × 2 mm pads at both ends for electrical access. The metal stripe resistance versus temperature measurements was calibrated for each metal stripe. Temperature was measured both by K-type thermocouple and by measuring the calibrated metal line resistance.

The 3ω signal acquisition was performed using a 12 bit DAC converter in the 10 Hz to 1 kHz range, using a four probe configuration. A 1 Ω shunt resistance in series with the metal line was used to monitor the current. The current amplitudes were kept in the 70–80 mA for all samples, ensuring a small mean temperature elevation (<2 K).

2.2. Validation on Si silicon substrate

In order to check the accuracy of the thermal conductivity measurements and analysis, we first used a p-boron (~10^{15} cm^{-3}) doped silicon substrate. A value of 148 ± 1 W/m K at 300 K is obtained, which is in very good agreement with previously reported values [14]. Fig. 1 shows the measured temperature rise as a function of twice the current frequency (2f), that confirms the good agreement of our measurements with the theoretical model of Borca-Tasciuc et al. [13] even at rather low frequencies. The temperature elevation at low frequencies due to the finite thickness (330 μm) of the Si substrate is well reproduced by the model.
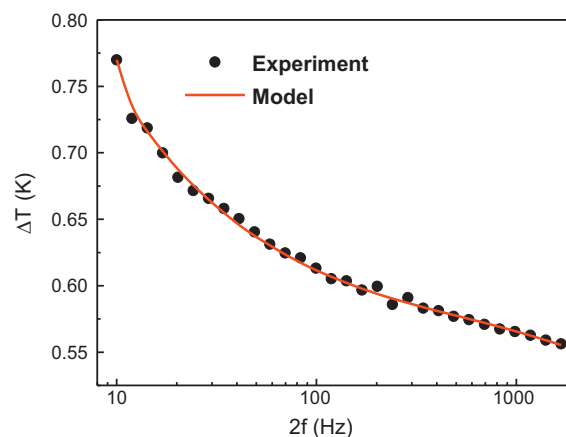

Fig. 1. 3ω method measured and modelled temperature elevation of a TiAu stripe on silicon substrate.

2.3. Thermal conductivity of InP n-doped substrate and SiN layer

A set of four InP, $n = 4 \times 10^{18}$ cm^{-3} S doped (1 0 0) commercial substrates from the same ingot (supplier: Sumitomo Corporation) was used. On each of them a SiN PECVD layer with different thicknesses varying from 100 to 600 nm was deposited in order to characterise both InP and SiN thermal conductivity, and the total TiAu/SiN/InP interface thermal resistance.

The thermal conductivity measurements on all substrates gave similar results with small differences (within 1 W/m K at each temperature). Fig. 2 represents the temperature dependence of the InP measured thermal conductivity. A fitting empirical power relation of the form $\lambda = A(T/300)^{-n}$ with $n = 1.57$ is deduced and found to be in good agreement with literature [15], but it is to be noticed that the A mean value at 300 K (75.6 W/m K) is slightly higher than those previously reported (68 W/m K [16] and 60.5 W/m K [15]) which could be due to a higher quality of currently available substrates.

The thermal conductivity of the SiN layer was also characterised and found to be 0.72 W/m K at room temperature. As shown in Fig. 3, the thermal conductivity slightly increases at higher temperature, which is a usual characteristic of SiN amorphous material. These values are in very good agreement with [17,18] for PECVD SiN layers. The thermal interface resistance (sum of the Ti–Au/SiN and SiN/InP interface resistances) was also deduced by measuring the variation of thermal resistance as a function of the SiN layer thickness on InP samples. Measurements are presented in Fig. 4. It was found to be 4×10^{-8} W/m^2 K which is comparable to previously reported values for SiN layers on Si samples [18].

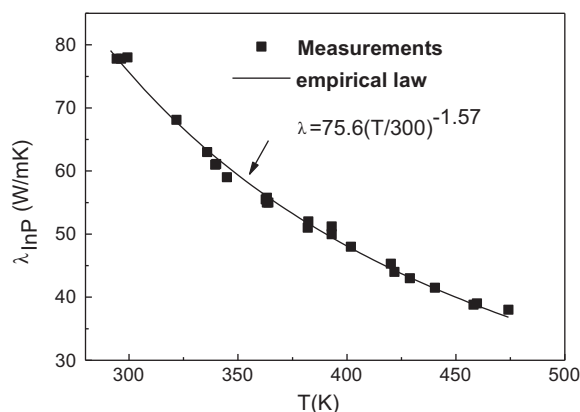**Fig. 2.** S-doped InP substrates measured thermal conductivity as a function of temperature.