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# Power devices in Polish National Silicon Carbide Program

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ABSTRACT

The paper is devoted to the Polish Government Program "New Technologies Based on Silicon Carbide for High Temperature, High Power and High Frequency Applications". The program consists of three general tasks, aimed at: SiC bulk and substrate material fabrication, SiC device manufacturing and SiC device applications, respectively. In the contribution the main assumptions and goals of the program are given, and the executed and evaluated part of the research is presented in the field of the design and manufacturing of SiC power semiconductor devices.



## 1. Introduction

For several years, the investigations dealing with the features of different silicon carbide polytypes as well as the technology of silicon carbide device manufacturing are more and more intensive. It is caused by the extremely attractive material parameters of silicon carbide in comparison to silicon ones, which is characterized by the larger band gap, the better heat conductivity, the larger electron saturation velocity and the larger critical electric field strength. These parameters, potentially, allow manufacturing silicon carbide devices with properties superior to the devices based on silicon or other semiconductor materials. The large critical electric field strength allows getting high voltage p–n junctions with the breakdown voltage larger than 10 kV. The large band gap makes possible manufacturing low noise devices or devices working at high temperatures exceeding even 700 °C whereas the large saturation electron velocity makes silicon carbide an excellent candidate for high-frequency devices with the possible maximal frequency reaching THz. The good thermal conductivity is very crucial from the reliability point of view (thermal stresses) and thermal management problems. The basic obstacle in practical use of silicon carbide in electronics consists in different, very often extreme, demands concerning the technology processes in comparison to the processes of silicon technology. It causes that the technology processes and characterization procedures well known in the silicon technology occur often to be inappropriate in the case of silicon carbide. The Polish National Silicon Carbide Program is aimed at solving some of these problems and it is expected that the results of its run will create the room for further activities towards the wider introduction of silicon carbide into electronics industry. It covers several research programs gathered in three tasks, realized by eight universities and three R&D units involved in SiC technology for several years.

## 2. Scope of the program

The structure of the program is shown in Fig. 1. It consists of three thematic tasks aimed at SiC bulk and substrate material fabrication, SiC device manufacturing and SiC device applications, respectively. Each of the tasks covers several partially complemented projects that are carried out by separate research teams coming from different research institutions. These institutions, listed in Table 1, gather the majority of Polish research groups engaged in the investigations in silicon carbide technology and application.

The first task is dominating in the program. Its main project is devoted to develop the technology of fabrication of 6H–SiC and 4H–SiC monocrystalline bulk material from silicon carbide powder using the methods based on Lelly approach. Other projects of this task concern next steps necessary to obtain 6H:SiC and 4H:SiC polished substrates with and without an epilayer, characterized by the quality satisfying device producers.

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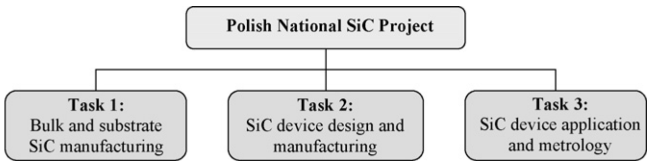


**Fig. 1.** Structure of the Polish National SiC Program.

**Table 1**
Research groups engaged in realization of Polish National SiC Program.

| |
|---|
| R&D units |
| Institute of Electronic Materials Technology, Warsaw |
| Institute of Electron Technology, Warsaw |
| Polish Science Academy, Warsaw |
| Universities |
| Warsaw University of Technology |
| University of Warsaw |
| Technical University of Lodz |
| Marie Curie-Sklodowska Lublin University |
| Wroclaw University of Technology |
| University of Wroclaw |
| Gdansk University of Technology |
| AGH University of Science and Technology, Krakow |

The second task involves projects dealing with different aspects of device manufacturing. Since the well characterized substrate is a base for any research activity aimed at semiconductor device manufacturing, a few projects is concentrated on the characterization methods specific for SiC structures, which are essential for the final results of technological processes. One of them concerns, e.g. the study of electrical, optical and photoelectrical characterization methods for MIS silicon carbide structures. Other projects deal with the technology problems like the technology of selective ion implantation, which is the key process for source and drain doping in MISFET technology as well as the termination in high voltage devices, the technologies of electrical contacts for silicon carbide devices and packaging technology taking also into account the problems resulting from silicon carbide application in high temperature electronics. In this task, the separate group is formed by the projects aimed at the manufacturing technology of particular devices with the final goal to deliver the demonstrators of these devices. They deal with Schottky diodes, PiN diodes, MISFET and JFET transistors manufactured on SiC substrates as well as with high-frequency HFET transistors and Schottky diodes manufactured as AIIIN AlN/SiC heterostructures.

The third task covers two projects only, concentrated on the investigations of advantages and disadvantages resulting from the application of SiC devices in power electronics circuits. Basing on the commercial available elements like Schottky diodes and MESFET transistors mainly, they cover the investigations of device features from the point of view of their influence on design process and work conditions in the power electronics equipment.

## 3. Investigations aimed at device development

### *3.1. Selective doping of silicon carbide*

The multiple energy aluminum implantations were performed at temperature of 500 °C into lightly doped ($5 \times 10^{15}\,cm^{-3}$) n-type, 10 μm thick epilayers grown on a heavily doped, 4° off-axis 4H–SiC substrate. Then, the samples were annealed at temperature of 1600 °C, pressure of 104 Pa, Ar flow of 90 l/min for 20 min. Surface roughness was examined using AFM across 5 μm × 5 μm areas. Channeled and rotating random RBS spectra were recorded to verify the amorphization degree. The amorphization degree was examined additionally by micro-Raman spectrometry with Ar laser (514 nm) and confocal microscopy imaging. The confocal imaging results are presented in Fig. 2 as a very effective way of radiation damages indication. Secondary ion mass spectrometry (SIMS) Al depth profiles was performed using a CAMECA IMS-6F prior to and after post-implantation annealing.

Hall measurements using van der Pauw configuration were performed after deposition of Ti/Al/Ti (10/60/30 nm) contacts and post-metallization annealing at 1050 °C for 1 min in Ar ambient. Implanted samples with highest aluminum concentration (2E19 $cm^{-3}$) demonstrated 20% activation level.

### *3.2. Thermal diffusion of dopants in SiC*

All the doping technologies that can be used for SiC PiN diodes fabrication require the high temperature processes. In the case of ion implantation doping, an additional annealing step is necessary after the main process of implantation to activate the introduced acceptor or donor atoms. Its temperatures are significantly large exceeding sometimes even 1600 °C. In the case of diffusion doping, the process can run successfully only when the temperature exceeds 1600 °C. Unfortunately, the temperatures exceeding 1600 °C evoke the sublimation process leading to destruction of the surface layer of processed SiC structure and in consequence, it can result in the damage of manufactured device. Therefore, it is of

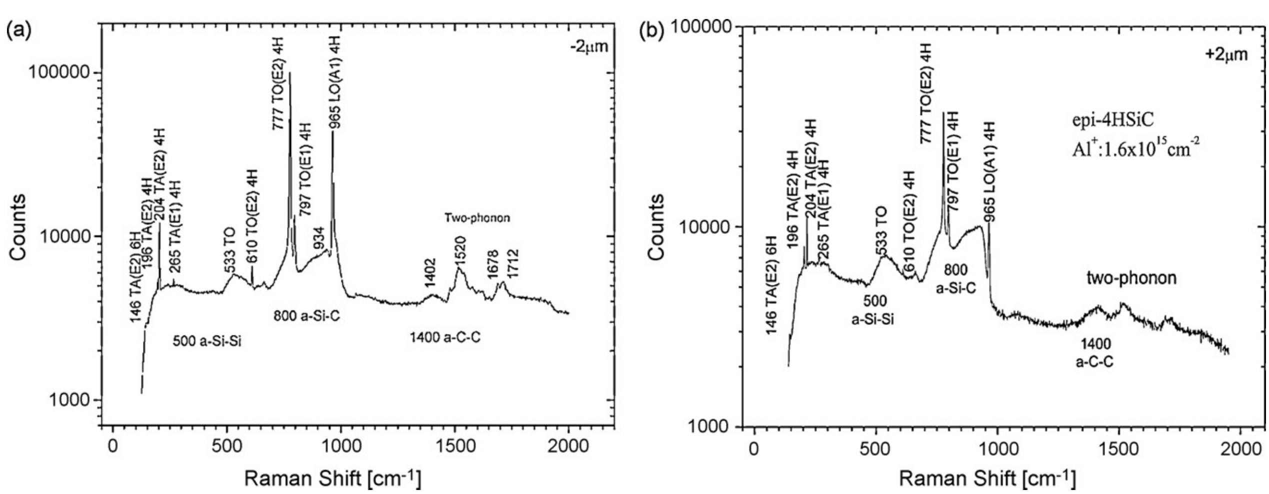


**Fig. 2.** Micro-Raman spectra of: (a) unimplanted epilayer and (b) Al-implanted epilayer.