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A neural approach to study the scaling capability of the undoped Double-Gate and cylindrical Gate All Around MOSFETs

F. Djeffal [a,*], M.A. Abdi [a], Z. Dibi [a], M. Chahdi [b], A. Benhaya [a]

[a] *LEA, Department of Electronics, University of Batna, Algeria*
[b] *LEPCM, Department of Physics, University of Batna, Algeria*

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Abstract

The Double-Gate and Gate All Around MOSFETs are two of the most promising candidates for the scaling of CMOS technology down to nanometer range. The excellent electrostatic control of the channel by the gate reduces dramatically short channel effects, such as charge sharing and DIBL. So, the objective of this work is to investigate and compare the scaling capability of the undoped DG and GAA MOSFETs using the artificial neural networks (ANNs). The optimization of this latter is based on the development of numerical models of subthreshold swing (S) for short channel Double-Gate and Gate All Around MOSFETs under various modes of operation based on a two-dimensional analysis of electrostatics in the channel region by solving the two-dimensional Poisson equation with the mobile charge term included, and apply the physical insights gained from these models to investigate the impact of process variations on device characteristics. This study leads to the conclusion that cylindrical geometry is superior to the equivalent Double-Gate structure both in terms of the electrostatic control of the channel and the current ratio I_{on}/I_{off}, indicating that the subthreshold slope is better controlled by the GAA MOSFET.
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1. Introduction

Multi-gate MOS transistors are widely recognized as one of the most promising solution for meeting the roadmap requirements for ultimate nanometer scale [1]. A wide variety of multi-gate architectures, including Double-Gate (DG), Gate All Around MOSFETs (GGA), have been proposed in the recent literature [2]. The Double-Gate MOSFET architecture is a potential solution to overcome short channel effects (SCE) in the 65-nm International Technology Roadmap for Semiconductors (ITRS) node [1,2]. The advantages advocated for DG MOSFETs include: ideal subthreshold slope; volume inversion [3] (for symmetric DG); setting of threshold voltage by the gate work function thus avoiding dopants and associated number fluctuation effects; etc. There are two main types of DG MOSFETs: (1) a symmetric type with both gates of identical work functions so that the two surface channels turn on at the same gate voltage and (2) an asymmetric type with different work functions for the gates and only one channel turns on at the threshold voltage [4]. The Gate All Around MOSFETs in which the gate oxide and the gate electrodes wrap around the channel region exhibit excellent transconductance and short channel behaviour because the strong confinement of the electric field from the Gate All Around the channel [5]. This device is particularly beneficial when it is used as a switching device in arrayed structures such as high-density dynamic random access memory (DRAM) and static random memory (SRAM) cells where a small device geometry and low leakage current are essential [6]. If the design parameters of GAA MOSFETs are optimized, it is expected that the short channel effects are adequately suppressed. Schematic representations of different multi-gate architectures are shown in Fig. 1.

Basing on the importance of these both architectures, in this paper we investigate the fully-depleted DG and GAA MOSFETs at miniaturization limits compatible with the 45 nm ITRS node and, in doing so, we tackle the coupled Boltzmann–Poisson equations within both a 2D box and a cylindrical domain. More specifically, we solve a 2D Poisson equation coupled with as many Boltzmann equations as the number of mesh points within the domain of modelling. Assuming a concept of effective conducting path [7], the numerical model explains the dependence

* Corresponding author. Tel.: +213 73796503; fax: +213 33 924540.
E-mail address: faycaldzdz@hotmail.com (F. Djeffal).

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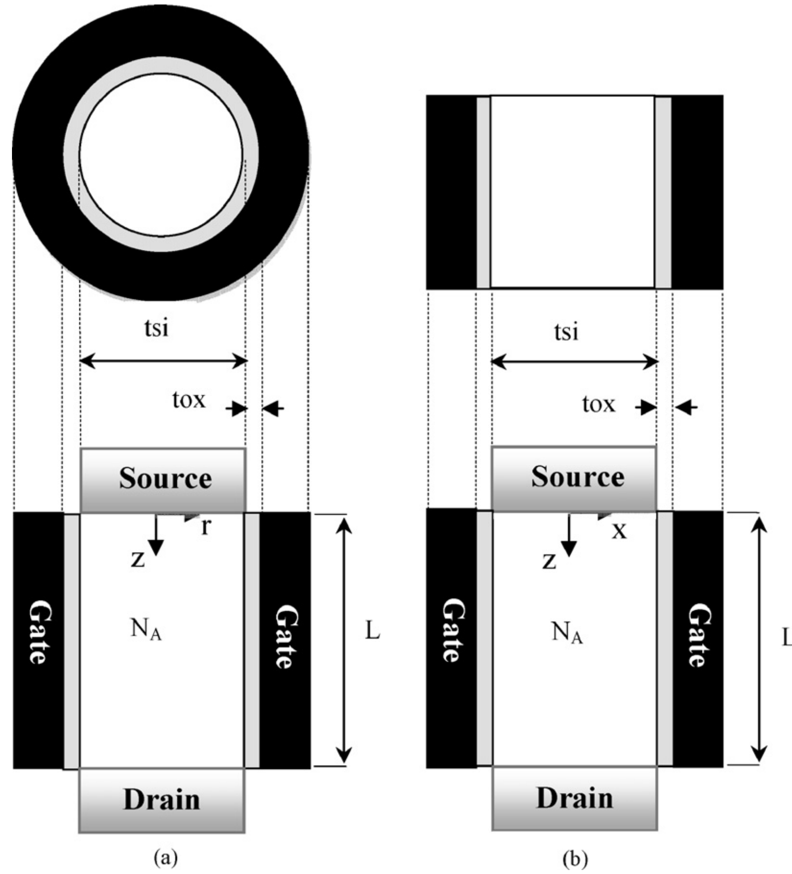

Fig. 1. Cross sections structures and coordinates. (a) Gate All Around and (b) Double-Gate structures are shown. Uniform channel doping and metal-like source/drain regions are used in all simulations.

of subthreshold swing (S) according to the doping of the channel and the effect of the various electrical and geometrical parameters. The database used for the optimization of the neural network is built based on a numerical model of the subthreshold swing (S) developed using the finite elements method (FEM). ANN structure obtained from this optimization will be used to study the scaling capability of both architectures DG and GAA MOSFETs.

2. Modelling mythology

2.1. Numerical computations

Refer to Fig. 1 by accounting for the angular symmetry of the GAA MOSFET, the Poisson equations for potential ϕ in the above structures take the form

$$\text{DG structure :}\quad \frac{\partial^2\phi}{\partial x^2}+\frac{\partial^2\phi}{\partial z^2}=\frac{q(N_A+n(x,z))}{\varepsilon} \tag{1}$$

$$\text{GAA structure :}\quad \frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\phi}{\partial r}\right)+\frac{\partial^2\phi}{\partial z^2}=\frac{q(N_A+n(r,z))}{\varepsilon} \tag{2}$$

where the electrostatic potential ϕ is referenced to the Fermi level. The free electron concentration n follows the classic Boltzmann distribution as $n = n_i\,\mathrm{e}^{(\phi-\phi_F)/V_T}$ where V_T is the thermal voltage (KT/q), n_i represents the intrinsic electron concentration and ϕ_F is the difference between the Fermi level and the electron quasi-Fermi level to account for the non-equilibrium condition, satisfying the following boundary conditions for both cases (DG and GAA):

DG structure:

$$\phi_F(0,x)=0 \tag{3a}$$

$$\phi_F(L,x)=V_{DS} \tag{3b}$$

GAA structure:

$$\phi_F(0,r)=0 \tag{4a}$$

$$\phi_F(L,r)=V_{DS} \tag{4b}$$

V_{DS} being the drain voltage.

The boundary conditions for ϕ are found by satisfying the continuity of both the potential and the normal component of the electric displacement at the Si/SiO_2 interfaces; and continuity of the potential at the source/drain sides:

DG structure:

$$\varepsilon_{ox}\frac{V_{Feff}-\phi(z,t_{Si/2})}{t_{ox}}=\varepsilon_{Si}\frac{\partial\phi(z,x)}{\partial x}|x=t_{Si/2} \tag{5a}$$

$$\varepsilon_{ox}\frac{V_{Beff}-\phi(z,t_{-Si/2})}{t_{ox}}=\varepsilon_{Si}\frac{\partial\phi(z,x)}{\partial x}|x=t_{-Si/2} \tag{5b}$$

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