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Epitaxial engineered solutions for ITRS scaling roadblocks

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Abstract

This paper reviews the current and future roles of epitaxy in providing both process and materials solutions to the scaling roadblocks identified by ITRS2005.

It is now widely accepted that we are in an "era of materials enabled device scaling" [International Technology Roadmap for Semiconductors, 2005 Edition, Front End Processing.] and that in addition to new materials for the gate stack, advanced substrates will also become increasingly important in the 21st Century. The Emerging Materials Committee has identified a range of issues such as mobility enhancement and thermal management [M. Bulsara, G. Celler, H. Huff, R. Standly, E. White, Solid State Technol. (2006).] which can be addressed by new "engineered" substrates that are now manufacturable thanks to combinations of advanced layer transfer and epitaxy processes.

Strained silicon has proved to be an invaluable performance booster due to the enhanced mobilities resulting from different forms of uniaxial and biaxial strain. SiGe epitaxy is the key process enabling technology for both process induced (local) strain and bulk (global) strain. Hybrid orientation technology (HOT), where (1 0 0) and (1 1 0) surfaces coexist on the same silicon substrate, is also an exciting development for boosting pMOS mobility. Several embodiments of this approach also exist and all require forms of epitaxial processing.

Advanced layer transfer processes make it possible to engineer substrates in a variety of ways which were, until recently, unimaginable. Layer transfer is essential to hybrid orientation technology and also makes strained silicon extendable onto SOI to produce ultra thin body (UTB) strained SOI substrates suitable for fully depleted CMOS devices.

In addition to its role in strain processes and engineered substrates, the number of 'in-process' epitaxy stages is also increasing. BiCMOS and HBT epitaxy are established technologies, however, the requirement to reduce source/drain series resistance is driving the introduction of elevated structures grown using selective epitaxy.

In summary, innovative epitaxy processes are essential for meeting the performance requirements of next-generation technologies and also have a crucial role in engineered substrate manufacture.

Keywords: Epitaxy; Strained silicon; Scaling; Engineered substrates; Raised source/drain; Thermal management; Mobility enhancement

1. Introduction

Epitaxy has become a key enabling technology for providing both materials and process solutions to several of the difficult scaling challenges identified by ITRS2005.

Until recently silicon epitaxy was used in just a few applications, these included BiCMOS where a silicon layer is grown directly above heavily doped collector regions and epitaxial starting substrates which are preferred to bulk silicon substrates due to their superior GOI (gate oxide integrity) performance [2] and latch-up immunity.

The advent of SiGe epitaxy then made it possible to engineer the band-gap and the lattice constant of the deposited film. Bandgap engineering of thin pseudomorphic SiGe and SiGeC films using low temperature epitaxy is now widely used for HBT (heterojunction bipolar transistor) devices and engineering of the lattice constant (through controlled grading of thicker SiGe films) enables the growth of strain relaxed buffer layers which can be used as templates for bulk strained silicon and even germanium.

New tool platforms developed to manufacture such demanding layers have resulted in exceptional levels of process control

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with respect to the key film parameters. These new capabilities have enabled integration of both selective and heterogenous epitaxy into leading edge, high volume manufacturing processes.

2. Role of epitaxy in mobility enhancement

Enhanced channel mobility is needed to improve saturated drive current (I_{DSAT}) and also to recover the mobility degradation resulting from the pending introduction of high-k gate dielectrics. Without strained silicon high-k transistors will have no performance improvement over transistors with conventional gate oxides [3]. The non-scalability of gate oxides and the current lack of a suitable high-k gate dielectric material have placed additional focus on strain techniques as a performance booster.

Several alternative approaches are being taken. Process induced strain was introduced into volume manufacturing at the 90 nm technology node by Intel. However, bulk strained silicon is still receiving significant attention because it remains the most promising route to sSOI (strained silicon on insulator) substrates. These will be needed to overcome the insurmountable short channel effects in future technology nodes.

3. Process induced (local) strain

The preferred method for inducing compressive strain in pMOS transistors is through low temperature, selective epitaxial growth of SiGe films into substrate recesses immediately adjacent to the channel. This same process stage can also be used to elevate the source/drain regions of the transistor and impart additional performance improvement by reducing the S/D series resistance (Fig. 1).

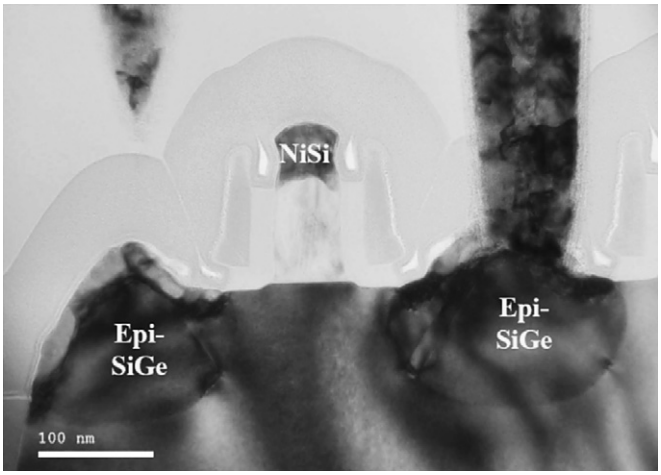

Fig. 1. Intel pMOS cross-section showing embedded SiGe. Ref. [4]. Dick James Chipworks Inc.

The cross-sectional SEM shows that the channel region is completely free of dislocation defects, though several can be seen at the edge of the embedded SiGe structure. An additional benefit of this approach is that the p-MOS transistor performance can be boosted independently of the n-MOS devices. This is not true of bulk strained silicon substrates which typically drive the n-MOS and p-MOS performance further apart due to the mobility enhancement for the electrons being far higher than the holes.

4. Bulk (global) strain

Bulk strained silicon proved difficult to integrate into volume production due to several reasons including the presence of high

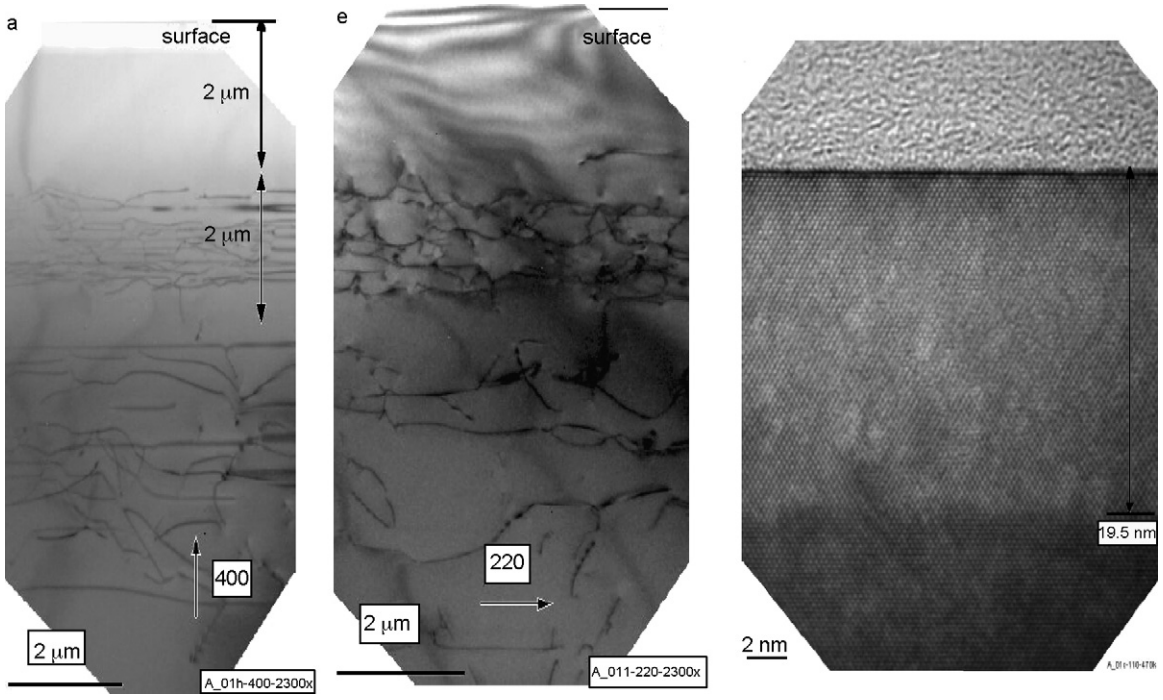

Fig. 2. Bulk strained silicon-XTEM showing confinement of dislocation network to the grade and a high quality silicon surface. Ref. IQE/Siltronic.