Materials Science and Engineering R 83 (2014) 1–59

Contents lists available at ScienceDirect

Materials Science and Engineering R

journal homepage: www.elsevier.com/locate/mser

Recent progress in resistive random access memories: Materials, switching mechanisms, and performance

F. Pan [*], S. Gao, C. Chen, C. Song, F. Zeng

Key Laboratory of Advanced Materials (MOE), School of Materials Science and Engineering, Tsinghua University, Beijing 100084, PR China

ARTICLE INFO

Article history:
Available online 10 July 2014

Keywords:
Resistive switching
Resistive random access memory
Nonvolatile memory
Memristor
Organic resistive memory

ABSTRACT

This review article attempts to provide a comprehensive review of the recent progress in the so-called resistive random access memories (RRAMs). First, a brief introduction is presented to describe the construction and development of RRAMs, their potential for broad applications in the fields of nonvolatile memory, unconventional computing and logic devices, and the focus of research concerning RRAMs over the past decade. Second, both inorganic and organic materials used in RRAMs are summarized, and their respective advantages and shortcomings are discussed. Third, the important switching mechanisms are discussed in depth and are classified into ion migration, charge trapping/de-trapping, thermochemical reaction, exclusive mechanisms in inorganics, and exclusive mechanisms in organics. Fourth, attention is given to the application of RRAMs for data storage, including their current performance, methods for performance enhancement, sneak-path issue and possible solutions, and demonstrations of 2-D and 3-D crossbar arrays. Fifth, prospective applications of RRAMs in unconventional computing, as well as logic devices and multi-functionalization of RRAMs, are comprehensively summarized and thoroughly discussed. The present review article ends with a short discussion concerning the challenges and future prospects of the RRAMs.

Contents

---

[*] Corresponding author. Tel.: +86 10 62772907; fax: +86 10 62771160.
E-mail address: panf@mail.tsinghua.edu.cn (F. Pan).

http://dx.doi.org/10.1016/j.mser.2014.06.002
0927-796X/

1. Introduction

Silicon-based Flash memories, consisting of a metal-oxide-semiconductor field-effect-transistor with an additional floating gate in each memory cell, represent the state-of-the-art nonvolatile memory and represent the lion's share of the current secondary memory market due to their high density and low cost. However, Flash memories suffer from several obvious disadvantages such as low operation speed (write/erase time: 1 ms/0.1 ms), poor endurance (10^6 write/erase cycles) and high write voltage ($>$10 V) [1]. Moreover, Flash memories will reach their miniaturization limit in the near future, not for technical reasons, but for physical limitations such as large leakage currents. To overcome the shortcomings of Flash memories, four emerging random access memories (RAMs) have been proposed: ferroelectric RAMs (FRAMs), magnetic RAMs (MRAMs), phase-change RAMs (PRAMs) and resistive RAMs (RRAMs). Among these memories, FRAMs and MRAMs also face the miniaturization issue because of their large memory cell size [1]. For PRAMs, the large power consumption during the reversible phase transition between the amorphous and crystalline phases would be the most serious obstacle to their commercialization [1]. Fortunately, RRAMs have been demonstrated to exhibit excellent miniaturization potential down to $<$10 nm [2] and to offer sub-ns operation speed [3,4], $<$0.1 pJ energy consumption [5,6] and high-endurance ($>10^{12}$ switching cycles) [7]. Therefore, RRAMs are also a potential alternative to the current main memory, i.e., dynamic RAMs (DRAMs).

In general, a RRAM cell is composed of a conductor/insulator (or semiconductor)/conductor sandwich structure, as shown in Fig. 1a. This simple structure enables it to be easily integrated in passive crossbar arrays with a small size of $4F^2$ (F is the minimum feature size), and the size can be further reduced to $4F^2/n$ within vertically stacked three-dimensional (3-D) architectures (n is the stacking layer number of the crossbar array) [8]. The intrinsic physical phenomenon behind RRAMs is resistive switching (RS), which means that the device can be freely programmed into a high resistance state (HRS, or OFF state) or a low resistance state (LRS, or ON state) under external electrical stimuli. In most cases, the current flows uniformly through the device in the HRS and is restricted to a local region with high conductance known as a conducting filament (CF) in the LRS [9]. The switching event from the HRS to the LRS and the corresponding voltage are denoted as set process and V_{set}, respectively. In contrast, the switching event from the LRS to the HRS and the corresponding voltage are denoted as reset process and V_{reset}, respectively. There are usually two types of switching modes: unipolar and bipolar switching. The former requires the same electrical polarity during the set and reset processes, whereas the latter requires opposite electrical polarities, as shown by the schematic current–voltage (I–V) curves in Fig. 1b and c, respectively.

It has been almost a half century since the initial experimental observations of RS. In 1962, Hickmott [10] observed large negative differential resistance in five thin anodic oxide films including SiO_x, Al_2O_3, Ta_2O_5, ZrO_2 and TiO_2. Subsequently, more materials were demonstrated to show RS, and the switching mechanisms started to be explored as well [11–13]. Strong research interest in RS, however, only lasted approximately a decade owing to the fact that the observed RS at that moment was not sufficiently robust for memory application, and also due to the prosperity of Si-based integrated circuit technology. Since the late 1990s, interest in RS began to revive because of the search for an alternative to Si-based memories. The first practical application of RRAMs was reported by Zhuang et al. [14]. These researchers fabricated a 64-bit RRAM array using $Pr_{0.7}Ca_{0.3}MnO_3$ via a 0.5-μm complementary metal-oxide-semiconductor (CMOS) process. The device showed good performance with low operation voltage ($<$5 V), fast speed ($\sim$10 ns) and a large memory window ($>10^3$). Meanwhile, organics-based RRAMs were introduced by Yang's group [15], greatly enriching the range of usable materials. In 2004, Baek et al. [16] successfully demonstrated the world's premier binary