Materials Science and Engineering R 72 (2011) 49–80

Contents lists available at ScienceDirect

Materials Science and Engineering R

journal homepage: www.elsevier.com/locate/mser

Threshold voltage shifting for memory and tuning in printed transistor circuits

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ARTICLE INFO

Article history:
Available online 31 December 2010

Keywords:
Organic Transistors
Memory
Threshold Voltage
Printed Electronics
Circuit Tuning
Charged Dielectrics

ABSTRACT

Multiple mechanisms for controllably shifting the threshold voltage of printed and organic transistors have been identified during the last few years, including some just in the past year, that are analogous in some ways to silicon floating gate memory elements. In addition, printed electronic memory is emerging as a serious product technology for identification and banking cards and for responsive systems through the efforts of startup companies. Other circuit applications are also being identified. Memory and tuning are not as prominently discussed in the literature as simpler and more accessible topics such as display driving, charge carrier mobility, voltage reduction, and high-frequency response. This report summarizes the numerous approaches being considered for the definition and control of transistor threshold voltage in alternative electronic technologies, including the theoretical basis for the effects utilized. Higher and more reliable performance parameters and entirely new functionality are among the advantages to be highlighted.

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0927-796X/$ – see front matter © 2010 Elsevier B.V. All rights reserved.
doi:10.1016/j.mser.2010.11.001

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1. Introduction and theoretical basis

Interest in the use of molecular materials for electronic applications has grown exponentially in the last two decades with ever increasing participation from academia, national labs, corporate labs, technology startups and consortiums of research institutions. The ability to manipulate organic molecules into functional assemblies with easy processing techniques that are scalable to mass production has given a major impetus to this field. Despite the fact that organic semiconductors would not be able to compete with the performance of traditional high quality inorganic semiconductors in high end applications, the potential advantages of organics in terms of cost, large area and low temperature processing, and large scale manufacturing on flexible substrates make them attractive candidates for certain applications and are already making inroads into emissive and non-emissive electronic displays. These advantages also bring new niche applications like flexible solar cells, white lighting, and printed memory into consideration.

For applications involving active circuits, organic field effect transistors (OFETs) are the devices at the heart of switching and logic operations. These devices utilize molecular solids and polymer films as the semiconductors. Charge transport in these media is largely via hopping among molecular-scale sites, with limited contribution from band-like transport in the purest and best ordered materials. While charge carrier mobilities are generally lower than for crystalline inorganic semiconductors, limiting switching frequencies and demanding higher voltages for similar current levels, additional tunability and function are enabled because of the atom-by-atom control of the semiconductor energy levels, heterogeneity, molecular orientations, and charge trapping sites. This atomic scale control particularly enables the tuning and adaptability of OFET threshold voltages, which opens up new possibilities for circuit fabrication and higher order functions such as energy capture and chemical sensing. The detailed analysis of OFET threshold voltage definition is the subject of this report.

1.1. Operation of field effect transistors

A transistor is essentially a resistor (with the two terminals called "source" and "drain" and a semiconductor as the resistive material) in combination with the metal–insulator–semiconductor (MIS) capacitor as shown in Fig. 1. A voltage applied on the gate terminal causes an accumulation of charge carriers in the semiconductor across the dielectric. The increase in the charge carrier density leads to increase in the conductivity of the 'resistor'. The device is thus called 'transfer resistor' or a 'transistor' because the resistance can be transferred from the gate terminal. Fig. 1 shows the schematic cross-sectional layout of an OFET.

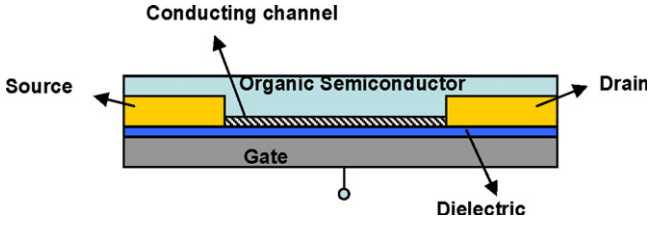

Fig. 1. Schematic view of an OFET.

The general operation of OFETs has been thoroughly described in earlier reviews, for example, by Horowitz [1–5], Sirringhaus [6], Zaumseil and Sirringhaus [7], Frisbie [8], and Katz [9]. In addition, many primary publications about OFETs include introductory explanations. The gate can be a conductive substrate (like highly doped Si) or a patterned electrode on an insulating substrate. The dielectric layer is either an insulating oxide (like SiO_2, Al_2O_3) or polymeric insulators (like poly(methyl methacrylate) (PMMA), polystyrene (PS), benzocyclobutene (BCB) polymer, or others) coated on the gate, with or without surface treatment. The patterned source/drain electrodes can be deposited prior to the organic semiconductor (OSC) evaporation or after it. The former case is a "staggered" configuration (popularly called bottom contact) and the latter is "coplanar" configuration (also known as top contact).

Without the application of the gate voltage V_g, the intrinsic conductivity of most organic semiconductors is low and so when a voltage V_d is applied between the two source–drain electrodes, very little current can flow through the semiconductor. In such a situation, the device is said to be in the 'OFF' state. By the application of a finite gate voltage V_g, there is a gradient in the potential across the dielectric and because of this there is a charge carrier accumulation at the dielectric–semiconductor interface. Ideally all of the accumulated charge would be free but in reality some of this charge is trapped, detracting from the charge available for transport. Since the conductivity is proportional to the number of mobile charge carriers, there is an order of magnitude increase in the current flow when a voltage V_d is applied between the source and drain electrodes, as a result of the gate voltage. In such a situation the device is said to be in the 'ON' state.

Fig. 2 shows the device characteristics of an OFET with pentacene as the OSC and the sodium-beta alumina, a high capacitance dielectric [10]. The left graph is a plot of increase in current with source–drain voltage for a certain voltage applied at the gate and is called the "output characteristics". The current increases linearly first with increase in source–drain voltage (linear region) and then saturates (saturation region). The plot on the right is the plot of current in the transistor as a result of variation in the gate voltage while the source–drain voltage is kept constant (−1 V here) and is called the "transfer characteristics". This curve is most often used to calculate different transistor parameters such as mobility and threshold voltage (V_t) that establish performance.

In the following, we shall give a quantitative description of current flow in OFETs and various associated device parameters starting from basic principles. As mentioned above, there are two aspects to a transistor operation to be considered: (a) the increase in charge carrier density in the channel as a result of the gate voltage application and (b) the transport of charge carriers from the source to drain electrode as a result of lateral source–drain potential difference. Most of the treatment has been previously mentioned in the classic text of Sze [235], Horowitz [4], Newman