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A 40 Gb/s InP-monolithically integrated DPSK-demodulator enhanced by cross-gain-compression in an SOA

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ABSTRACT

We fabricated and experimentally tested a novel monolithically integrated Indium Phosphide optical circuit for differential phase-shift keying demodulation, which is robust to noise degradations of the received signal. The circuit consists of a one-bit-delay interferometer that demodulates the incoming signal and a semiconductor optical amplifier where the constructive and destructive demodulated outputs synchronously counter-propagate experiencing a reshaping effect. The novel optical circuit has been fabricated for 40 Gb/s signals, and the amplitude signal restoration is demonstrated by comparing the obtained output eye diagrams with those of a commercial fiber-based demodulator. We find a net improvement in the signal to noise ratio when the circuit is fed with a noisy input signal.

1. Introduction

Differential phase-shift keying (DPSK) is an alternative modulation format with potential advantages for optical communication systems in terms of sensitivity and robustness to nonlinear impairments. Since the information is encoded in the optical phase change between adjacent bits, the receiver requires a differential demodulation in order to detect the phase information. Aim of the DPSK demodulator is to compare the incoming signal and its one-bit delayed copy, operation that is typically realized by means of a delay interferometer, to whose output port the consecutive bits interfere constructively, resulting in high optical power, or destructively, resulting in low optical power [1]. Commonly, DPSK demodulators exploit one-bit delay interferometers and are realized with all-fiber structures or silica planar lightwave circuits (PLCs). Other approaches use free space optics interferometers, hybrid Silicon on Insulator circuits or polymer PLCs [2–6]. Here we introduce a novel Indium Phosphide (InP) monolithically integrated demodulator for DPSK communication systems, which provides DPSK demodulation and amplitude restoration on both the constructive and the destructive demodulated outputs [7]. Even if not implemented in this first photonic integrated circuit (PIC) sample, this scheme allows for the monolithic integration of the demodulator with a balanced photodetector.

The PIC has been fabricated exploiting JePPIX [8], the European platform for the manufacturing of Indium Phosphide-based photonic integrated circuits. The platform pushes a generic integration technology, where standardized building blocks and foundry process are enforced, without technologies specifically developed or optimized for a given application.

2. Device description and operation principle

As sketched in Fig. 1, the PIC consists of a first DPSK demodulator stage made by an interferometer in which the incoming signal bit interferes with the previous one after being delayed in the one-bit delay loop, and a second regenerative stage realized by means of a saturated SOA. Fig. 1a and Fig. 1b show the scheme of the DPSK demodulator and a picture of the fabricated device.

A 2×2 Multi Mode Interference (MMI) coupler connects the arms of the interferometer to the Input and Monitor ports of the device. The optical delay line (ODL) provides a delay equal to the bit period (25 ps), suitable for 40 Gb/s signals. The two outputs of the demodulator, p1 and p2 (see Fig. 1), are connected through equal-length paths to the SOA and to their corresponding Output ports by means of two 2×1 MMIs. We remark that an integrated configuration simplifies the polarization management within the demodulator compared to bulk fiber-based implementations. The

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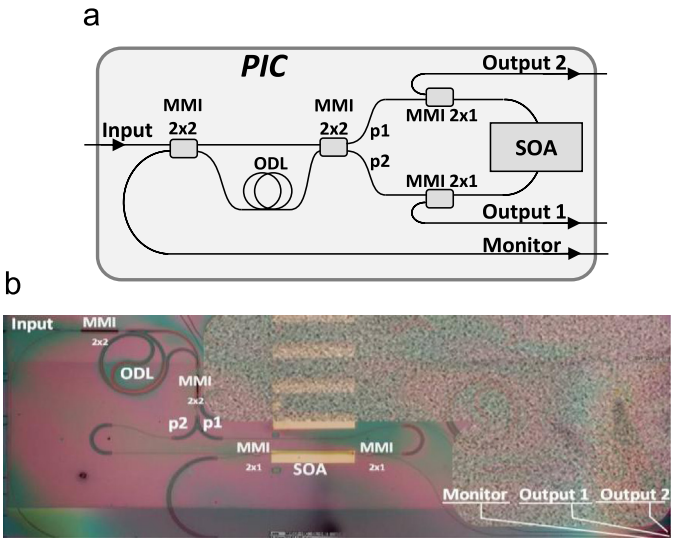

Fig. 1. Scheme of the DPSK demodulator (a); picture of the fabricated PIC (b).

SOA is 500 μm-long and has a measured small signal gain of 10 dB at a saturation current of around 70 mA. Proper tapers are used at any transition between the high-contrast waveguides used for the tightly curved sections of the circuit (corresponding to the thicker lines in Fig. 1b) and the low-contrast waveguides (the thinner lines in the picture). The effective refracting indices are in the order of 3.25 at 1550 nm wavelength for the shallow waveguides and of 3.19 for the deeply etched waveguides. In order to reduce optical reflections, the waveguides at the input and at the output of the chip are 7° angled with respect to the facets.

The working principle is as follows: the bit that enters the device from the Input port is split by means of the first 2×2 MMI coupler into two parts: half of the power enters the optical delay line, while the other half goes straight through the upper waveguide. After being one-bit delayed, each bit in the loop enters a second 2×2 MMI coupler, which combines the signals from the two interferometer arms. If the interfering symbols present equal phases, the output signal is maximized on the upper MMI output port (p1 in Fig. 1) due to constructive interference and minimized on the lower port (p2 in Fig. 1) due to destructive interference, otherwise, in case of different phases, high power appears on p2, and low power on p1. The two demodulated and logically inverted signals, after crossing a 2×1 MMI, are guided through equal-length paths to the opposite sides of the SOA where they counter-propagate, sharing its saturated gain. In this way, since a logical "one" and a logical "zero" always propagate at the same time into the SOA, signal level compression is obtained of both logical-one and logical-zero levels, and, consequently, the two signals experience a reshaping effect [9,10]. The demodulated data streams then cross the 2×1 MMI along their optical path and reach the corresponding device output ports.

3. Experiment and results

The experimental setup is sketched in Fig. 2. We generated a 40 Gb/s DPSK signal at wavelength 1551.7 nm by modulating a tunable continuous-wave laser with a Mach–Zehnder intensity modulator driven by a 2^{31}-1 pseudorandom bit sequence. The signal was combined with amplified spontaneous emission (ASE) noise from an Erbium doped fiber amplifier (EDFA) source after crossing a band pass filter (BPF) centered at the signal wavelength and a variable optical attenuator. An EDFA, a BPF, and a polarization controller (PC) are utilized to properly set the optical power and the polarization of the waveform before coupling it into the PIC. The total optical power at the PIC input port was 10 dBm, and the SOA driving current was around 100 mA. Tapered fibers were used to couple light to and from the InP chip having around 4 dB insertion losses per facet. Since each MMI introduces additional 1.5 dB of loss, and propagation loss is measured to be 3.0 dB/cm for the low-contrast waveguides and 4.6 dB/cm for the high-contrast waveguides resulting in around 1.5 dB of additional loss in the delayed path and 0.5 dB in the direct path, we can estimate the optical power at the SOA input to be around 1.5 dBm and 2.5 dBm for the two decoded signals entering the SOA, respectively. Fig. 3a shows the fiber-to-fiber input/output power characteristics measured on a test SOA on the same chip, showing the hard-limiting behavior of the SOA when fed with an optical power higher than 4 dBm. The signal collected from the PIC passed a BPF after being amplified by a further EDFA and was then detected by a sampling oscilloscope with a 50 GHz optical head. Eye diagrams of the input signals and of the constructive and destructive output signals are reported as insets of Fig. 2 in the case without noise loading, showing the effectiveness of the device. The spectra of the modulated signal at the PIC input port, and of the demodulated signal collected at output ports are also shown in Fig. 3b and c, respectively.

As bit error rate measurements were not possible due to the mechanical instability of the PIC fiber coupling, we analyzed the eye diagrams of the 40 Gb/s DPSK signal demodulated with our novel integrated InP demodulator comparing them with the ones obtained using an all-fiber commercial DPSK demodulator. We

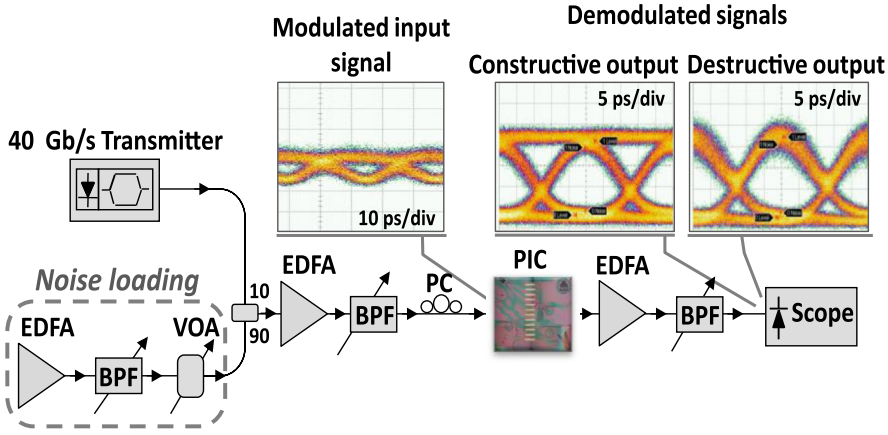

Fig. 2. Experimental set-up. Inset: eye diagrams of the input and the demodulated signals without noise loading.