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Design and characterization of a 30-GHz bandwidth low-power silicon traveling-wave modulator



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ABSTRACT

We present the design and characterization of a silicon PN junction traveling-wave Mach–Zehnder modulator near 1550 nm wavelength. The device shows 30 GHz bandwidth at 1 V reverse bias, with a 2.7 V-cm $V_{\pi}L_{\pi}$ and accordingly a 9-V small-signal V_{π} . The insertion loss of the phase shifter is 3.6 dB ± 0.4 dB. The device performance metrics in combination show significant improvement compared to the state-of-the-art in the sense that lower phase shifter loss and higher bandwidth are achieved for the same V_{π} or vice versa. We demonstrated low modulation power of 640-fJ/bit at 40 Gb/s with a 1.6- $V_{\rm pp}$ differential-drive and 0-V DC bias, raising the prospect of direct compatibility with CMOS drive-voltages. Critical design tradeoffs are analyzed and design models are validated with measurement results. We proposed a new figure-of-merit (FOM) $V_{\pi}L_{\pi}R_{\rm pn}C_{\rm pn}^2$ as the junction design merit for high-speed traveling-wave modulators, and utilized 6 implants to achieve an optimal FOM with lower insertion loss. Several key RF design issues are addressed for the first time using simulation and measurement results. In particular, we discussed bandwidth extension using mismatched termination and closely matched experimental results. A bandwidth-limiting RF multi-mode behavior is noted, which also exists in other results in the literature; we suggested a widely applicable design remedy.

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1. Introduction

Silicon optical modulators [1] are critical for data communication related applications [2–5] in silicon photonics. Over the past decade, significant progress has been made in this area, but achieving efficient high-speed modulation in silicon still proves to be challenging, mainly due to the weak electro-optic (EO) effects available in this material [5,6].

The fundamental and key modulator device metrics include insertion loss, device bandwidth, and EO modulation efficiency (for Mach–Zehnder modulators the efficiency is characterized by V_{π}). In addition, optical bandwidth, device footprint, temperature sensitivity, fabrication error tolerance and CMOS compatibility are also of great importance for practical designs, design scalability and possibility of CMOS monolithic integration [7,8].

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http://dx.doi.org/10.1016/j.optcom.2014.01.071 0030-4018 © 2014 Elsevier B.V. All rights reserved. A majority of the high-speed demonstrations thus far have been based on reverse-biased silicon PN junctions. Among these results, high-speed resonator modulators are promising in achieving ultra-low modulation power consumption and compact device footprint. Recently, Li et al. demonstrated a 40 Gb/s 1 V-drive ring modulator [9], although a few issues remain to be fully addressed, such as limited optical bandwidth, and consequently necessary thermal drift stabilization as well as operating wavelength alignment between devices.

The other main category of carrier-depletion PN junction modulators is traveling-wave Mach–Zehnder (TWMZ) modulators. Although in academic demonstrations imbalanced Mach–Zehnder (MZ) modulators are often used (mostly for the convenience of testing), balanced MZ modulators are the true practical devices and have the key advantage of being temperature insensitive, thus do not require active thermal stabilization. Traveling-wave design enables the driving of a long phase-shifter at high speed, therefore can yield low voltage modulators.

40–60 Gb/s channel speed is a logical next step from existing 25–28 Gb/s data rates. The device we present here targets at

applications at these speeds or equivalently a device bandwidth of approximately 30 GHz [9–11]. In recent TWMZ results [10–15] however, it was often found that a similar bandwidth was only achieved with very short devices (\sim 1 mm or less) as well as high bias voltages (frequently 3–5 V), both of which limit the modulation efficiency. High V_{π} and associated high drive voltages increase power consumption and make the devices less compatible with advanced CMOS, which is usually constrained by low-breakdown voltages. For long devices [14,15], in addition to smaller bandwidth, they were demonstrated with high insertion loss on the phase shifter making it difficult to fit in a practical system link budget. In summary, further device improvements remain to be made for high-speed low voltage modulators with low loss.

In this paper, we present a 3-mm long, 30-GHz bandwidth differential-drive silicon TWMZ modulator based on a lateral PN junction with low reverse bias. The phase shifter $V_{\pi}L_{\pi}$ is 2.7 V-cm (a small-signal V_{π} of 9 V) and the insertion loss on the phase shifter is only 3.6 dB. At similar bandwidth this device shows the lowest V_{π} and lowest drive voltage requirement due to differential-drive, or at similar V_{π} it shows the highest bandwidth as well as the lowest insertion loss on the active phase shifter [10–15]. The combined device metrics show significant improvement compared to the state of the art. The main part of the paper is organized as the following. Section 2 describes the fabrication process, identifies key design tradeoffs and presents design details of the device. Section 3 presents the measurement results, compares them to simulation results to validate the design model and provides discussions about several RF effects regarding TWMZ design that were not addressed in previous publications.

2. Device design and fabrication

2.1. Fabrication process

Aluminum

Air

Oxide

The device presented in this work was fabricated at the Institute of Microelectronics (IME)/A*STAR [17] through an OpSIS Multi-Project Wafer (MPW) run [18]. The fabrication process was very similar to that in [16] with the main difference being that in this work we employed six implant layers instead of four in silicon, and they were: lightly doped P and N for forming the junction in the waveguide core, intermediate density P+ and N+ for reducing series resistance without inducing excessive optical loss, and heavily doped P++ and N++ implant for low resistance silicon far away from the waveguide and for forming low resistance metal-to-silicon contact - no silicidation was used in the fabrication process, the contact was formed directly between aluminum and heavily doped silicon. The traveling-wave phase shifter crosssection is illustrated in Fig. 1 and the microscope photo of the fabricated device is shown in Fig. 3(b). The wafer was an 8" Silicon-on-Insulator (SOI) from SOITEC with 220 nm top silicon,



High-resistivity substrate (750 Ohm-cm)



Fig. 2. Schematic of the simplified equivalent circuit of the PN junction loaded transmission line.

 $2 \,\mu\text{m}$ buried oxide layer and 750 Ω -cm high resistive silicon substrate. The silicon slab thickness was 90 nm and ridge waveguide width was 500 nm. The top metal Aluminum was used for the traveling-wave electrodes, and it was 2 μ m thick, mostly situated above dielectric materials in the back-end stack. Other metal and dielectric material properties and thicknesses as well as fabrication steps were identical as they were in [16].

2.2. Overall device design considerations

In this section we briefly review the TWMZ design model and present useful design tradeoff relations to facilitate further discussions in this paper. The cross-section of the TWMZ shown in Fig. 1 is considered as a PN junction loaded transmission line and its equivalent circuit model is schematized in Fig. 2. $R_{tl}(f)$ is the frequency-dependent metal skin resistance in Ω/m , and has a \sqrt{f} dependence in principle, C_{tl} and L_{tl} are the capacitance and inductance between the metal traces in the units of F/m and H/m respectively. C_{pn} is the PN junction capacitance (in F/m); the total amount of silicon series resistance from the electrodes to the edges of the junction depletion region is captured in R_{pp} (in Ω -m). We further define the junction intrinsic RC bandwidth as $f_{rc} = 1/(2\pi R_{pn}C_{pn})$ and approximate the device impedance as $Z_{dev} = \sqrt{L_{tl}/(C_{tl}+C_{pn})}$, which is accurate when the frequency is well below the intrinsic RC bandwidth, i.e. $f/f_{rc} \ll 1$. It is worth nothing that, due to the use the high-resistivity substrate, the substrate conductance due to transverse current flow can be neglected in the frequency range of interest [29].

The bandwidth of a TWMZ modulator is mostly determined by the RF loss due to R_{pn} , if RF and optical velocities are closely matched. To make this clear we can look at the overall RF field loss coefficient (in the unit of Neper/m), which can be expressed as [19]

$$\alpha = \alpha_{metal} + \alpha_{silicon}$$

$$\approx \frac{1}{2} \frac{R_{tl}(f)}{Z} + \frac{2\pi^2 f^2 R_{pn} C_{pn}^2 Z_{dev}}{1 + 2\pi^2 f^2 R_{pn} C_{pn}^2 Z_{dev}}$$
(1a)

 $\overline{2} \overline{Z_{dev}}^+$

 $1 + (f/f_{rc})^2$

$$=\frac{1}{2}\frac{R_{tl}(f)}{Z_{dev}} + \frac{\pi f^2 C_{pn} Z_{dev}}{f_{rc}(1 + (f/f_{rc})^2)}$$
(1b)

Where α_{metal} and $\alpha_{silicon}$ are the loss due to metal series resistance and lateral silicon resistance respectively. Let us refer to the first term as R_{tl} loss and the second term as R_{pn} loss. At high frequencies, the second term usually dominates because of its f^2 dependence, whereas $R_{tl}(f)$ has a \sqrt{f} dependence. Incidentally, this can be seen clearly in Fig. 4(g), a simulation plot of the actual device under discussion.

For the moment, let us assume perfect velocity match and neglect other non-ideal RF effects (such as reflection, multi-modal behavior etc.), a straightforward relation between EO 3dB bandwidth $f_{EO,3 \text{ dB}}$ and achievable device length L_{dev} can be derived as [20]:

$$\frac{1 - e^{-\alpha(f_{EO,3 dB})L_{dev}}}{\alpha(f_{EO,3 dB})L_{dev}} = \frac{1}{\sqrt{2}} \Rightarrow \alpha(f_{EO,3 dB})L_{dev} = 0.74Neper = 6.4 \text{ dB}$$
(2)

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