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Controlled doping of graphene using ZnO substrates

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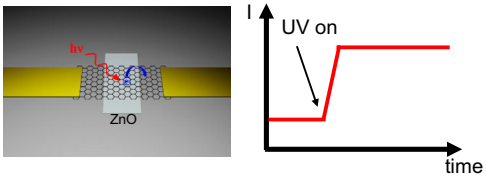
HIGHLIGHTS

- Graphene device could be doped by atomic layer grown ZnO on SiO_2 substrate.
- Graphene devices on ZnO layer show marked difference from those on SiO_2 substrates.
- Bottom ZnO atomic layer behave as an electron donor.

GRAPHICAL ABSTRACT

In graphene devices supported on ZnO film, ZnO layer behave as an electron donor. UV illumination experiment on hybrid graphene-ZnO device reveals that the effect of doping from ZnO becomes dominant when ZnO stripe width made larger than that of the graphene channel.



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ABSTRACT

We show that graphene device could be controllably doped by the bottom substrate by inserting atomic layer deposition grown ZnO between graphene and SiO_2 substrate. To clarify the effect of bottom ZnO, length of the graphene transistor channel was varied from 20 to 200 μm, while that of ZnO was fixed to 10 μm. Graphene devices supported on ZnO film show marked difference from those supported on SiO_2 substrates; bottom ZnO layer behave as an electron donor. UV illumination experiment on hybrid graphene-ZnO device reveals that the effect of doping from ZnO becomes negligible when the graphene channel length made about four times larger than that of ZnO stripe.

Graphene is one atom-thick, ideal 2-D material under intensive scientific research [1]. Graphene has many exiting physical and chemical features, many of them closely related with its one atom-thinness. Transparency of graphene is of particular interest, since the optical transparency of graphene is coming from its thinness, not related with its band structures [2]. In that sense, graphene could be transparent toward many other types of interaction. For example, Jeong et al. showed that graphene is transparent for electron-transfer interaction, by performing a galvanic displacement of noble metal ions on graphene supported on reducing substrate [3]. Wetting transparency of graphene has reported by several research groups [4–6], and Wang et al. showed that spatial patterning of chemical reactions on graphene surfaces by utilizing the underlying substrate [7]. In the context of such results, SiO_2 substrates that contains many defects and pinholes are not recommended, but hexagonal boron nitride (hBN) or free-standing graphene is recommended for studying the intrinsic properties of graphene, or to fabricate high performance devices. Yet, stated reversely, such substrate-sensitivity of graphene could be utilized to engineer electrical properties of graphene.

In this work, we use atomic layer deposition (ALD) grown ZnO as a dopant to change the electrical properties of graphene. Metal oxide such as ZnO or TiO_2 are the most widely used semiconducting materials hybridized with graphene; multi-functionality could be obtained from metal oxides to fabricate *p-n* junctions [8], solar cells

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[9,10], catalysts [11,12], field emission devices [13] and sensors [14–16] etc. Yet, quantitative analysis regarding the effect of metal oxide on graphene is rather primitive up to now.

Graphene has synthesized using chemical vapour deposition (CVD) on 25 μm-thick Cu foil (Alfa Aesor). Prior to graphene growth, Cu foils were slightly etched using Ni etchant (Transene, TFB), and thoroughly washed. Cleaned Cu foil was heated to 1000 °C under 100 sccm H_2 for 20 min, and precursor CH_4 (30 sccm) carried by H_2 (30 sccm) was introduced for growth. The growth was carried out for 40 min and then cooled to room temperature in vacuum. The graphene grown Cu foils were coated with PMMA (950K, 4% volume dissolved in chlorobenzene) at 3000 rpm for 30 s, and dried at RT for 2 hrs. The Cu foil with PMMA-coated graphene was etched using a cold copper etchant (Transene, CE-100) and then washed with clean DI water for 3 times. Suspended PMMA-coated graphene film was transferred onto the desired substrate, and then dried at RT for more than 2 hrs. Finally, PMMA layer has removed with warm Aceton. The ZnO thin films were made by ALD in a Lucida D-100 chamber using diethylzinc (DEZ, electronic grade; Sigma-Aldrich, MO, USA) and H_2O as the reactant and oxidant respectively. ZnO deposition was performed with DEZ-purge-H_2O-purge cycles controlled at 0.5 s-10 s-0.1 s-30 s sequences repeatedly, and the temperature was fixed at 150 °C. 100 nm-thick ZnO thin film has made with 500 cycles of ALD.

In order to fabricate hybrid ZnO-graphene film devices, following fabrication scheme has used. Fig. 1 shows schematic diagram of the hybrid device fabrication. First, ~ 100 nm thick ZnO films were grown on oxidized silicon substrate by atomic layer deposition (ALD). Electrical contacts were made on them by photolithography and thermal evaporation of Cr and Au. These electrical contact pads act as alignment markers for subsequent lithography steps. Bottom ZnO strips were made by another photolithography step and wet etching with dilute HNO_3. Then, CVD grown monolayer graphene has transferred onto the substrate with electrical contact pads and ZnO strips, then patterned so that the graphene channel could be created. In order to analyze the effect of ZnO, graphene channel length has varied from 20 to 200 μm while the width of bottom ZnO stripe has fixed as 10 μm. As a control experiment, we have fabricated graphene transistor devices and ZnO thin film devices as well. Fig. S1 in Supporting Information shows optical microscope image and AFM image of a typical graphene device and its Raman spectrum.

Fig. 2(a), (b), and (c) show gate transfer characteristics of hybrid graphene devices with (a) 20 μm, (b) 40 μm and (c) 200 μm channel graphene devices with 10 mV source–drain bias voltage. The source–drain bias voltage was 10 mV for the all measurements. Fig. 2(d)–(f) correspond to their transfer characteristics in vacuum. Normally, graphene devices fabricated on oxidized silicon substrate show heavily *p*-doped behavior, Dirac point located at far positive gate voltages. Dirac point is not discernable in the pristine graphene device shown in Supporting Information Fig. S2 even with 100 V gate bias voltages in the ambient condition. While Dirac point of 200 μm-long graphene device locates around ~ +80 V, those of 20 and 40 μm graphene devices locate near zero gate bias. Since ZnO is an *n*-type semiconductor, electrons from ZnO will be transferred to graphene. Also, gate hysteresis behavior shows marked difference depending on the ratio between graphene channel length and ZnO channel width. 20 μm-long graphene device shows the largest hysteresis, and gradually decreases with increasing graphene channel length. It is also interesting to note that such gate hysteresis even persists in vacuum conditions when graphene channel length/ZnO width is smaller than 4. Normally, graphene devices constructed on SiO_2 substrate show relatively large hysteresis in ambient conditions, but hysteresis disappears upon evacuation; it is thought that the hysteresis is coming from water molecules trapped in graphene-SiO_2 interfaces, which disappears upon evacuation. However, as shown in Fig. 2(d), hysteresis persists even in vacuum conditions for short channel graphene devices. Since ZnO may also be electrostatically doped using back-gate, it is understandable that graphene devices show gate hysteresis behavior even in vacuum conditions. And such pronounced gate hysteresis in vacuum has only observed in short (20 μm) channel graphene device. As the channel length of graphene increases, it became more resistive especially for polycrystalline CVD graphene that contains large number of defects. Therefore, pronounced hysteresis in vacuum conditions is only observable in short channel hybrid devices.

Next, responses of hybrid devices upon UV illumination has explored with hybrid devices with different channel lengths as shown in the Fig. 3. For the experiment, we have used 120 W Xenon fiber optic light source (broadband output from 200 to 1100 nm) connected with the vacuum chamber. Normally, graphene devices show decrease of conductance under UV light, since UV illumination causes desorption of oxygen molecules bound on graphene or contact electrode. For *p*-type graphene devices, oxygen removal appears as *n*-doping, conductance decreases accordingly as shown in as shown in Fig. 4(a) in ambient condition. On

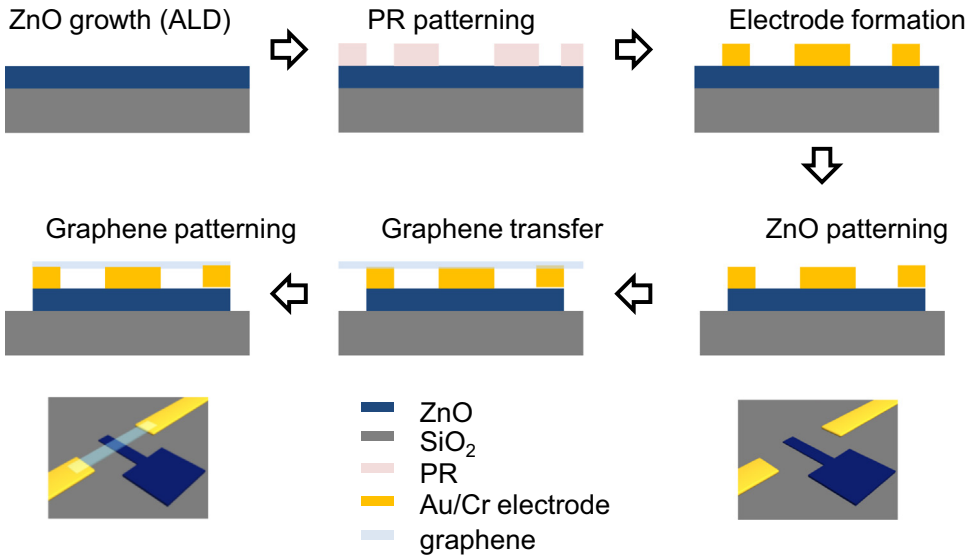

Fig. 1. Schematic of the hybrid device fabrication.