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# Novel Indium Arsenide double gate and gate all around nanowire MOSFETs for diminishing the exchange correlation effect: A quantum study

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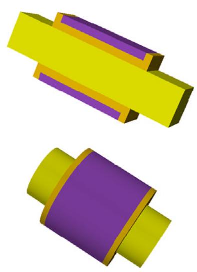
## HIGHLIGHTS

- DG-MOSFET and GAA-NWT are presented with diminished exchange-correlation effect.
- The key idea in this work is to use InAs semiconductor instead of Si.
- Quantum mechanical transport approach based on NEGF has been performed.
- A few lowest Eigen sub-bands are occupied and the upper sub-bands can be safely neglected.
- Interaction between electrons and Ex-Corr effect is diminished in the proposed structure.

## GRAPHICAL ABSTRACT

The key idea in this work is to use Indium Arsenide (InAs) semiconductor instead of Si for diminishing the exchange-correlation (Ex-Corr) effect.



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## ABSTRACT

In this paper we present novel double gate (DG) metal oxide semiconductor field effect transistor (MOSFET) and gate all around (GAA) nanowire metal oxide semiconductor field effect transistor (NWT) with a diminished exchange-correlation (Ex-Corr) effect. The key idea in this work is to use Indium Arsenide (InAs) semiconductor instead of Si. We have evaluated and compared different parameters of DG-MOSFET and GAA-NWTs such as threshold voltage, sub-threshold slope, drain induced barrier lowering and ON and OFF state currents from quantum view. Quantum mechanical transport approach based on non-equilibrium green's function (NEGF) has been performed in the frame work of effective mass theory in consideration with Ex-Corr effect. This simulation method consists of three dimensional Poisson's equation in which a Schrodinger equation is first solved in each slice of the device to find Eigen energies and Eigen functions. Then, a transport equation of electrons moving in the sub-bands is solved. This fully quantum method treats such effects as source-to-drain tunneling, ballistic transport, and quantum confinement on equal footing. The results show that only a few lowest Eigen sub-bands are occupied and the upper sub-bands can be safely neglected. Also, the interaction between electrons and Ex-Corr effect is diminished in the proposed structure.



## 1. Introduction

As the channel length becomes smaller and smaller, short channel effects (SCEs) occur and becomes more significant in metal oxide semiconductor field effect transistors (MOSFETs). At the same time, the relatively low carrier mobility in silicon

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(compared with other semiconductors) may also degrade the MOSFET performance (e.g., ON-current and intrinsic device delay). For these reasons various novel device structures and materials are being extensively explored. Non classical structures like double gate (DG) and gate all around (GAA) MOSFET transistors are invented to overcome SCEs in nanometer-regime MOSFETs [1,2]. The DG and GAA devices ensure that no part of channel is far away from the gate.

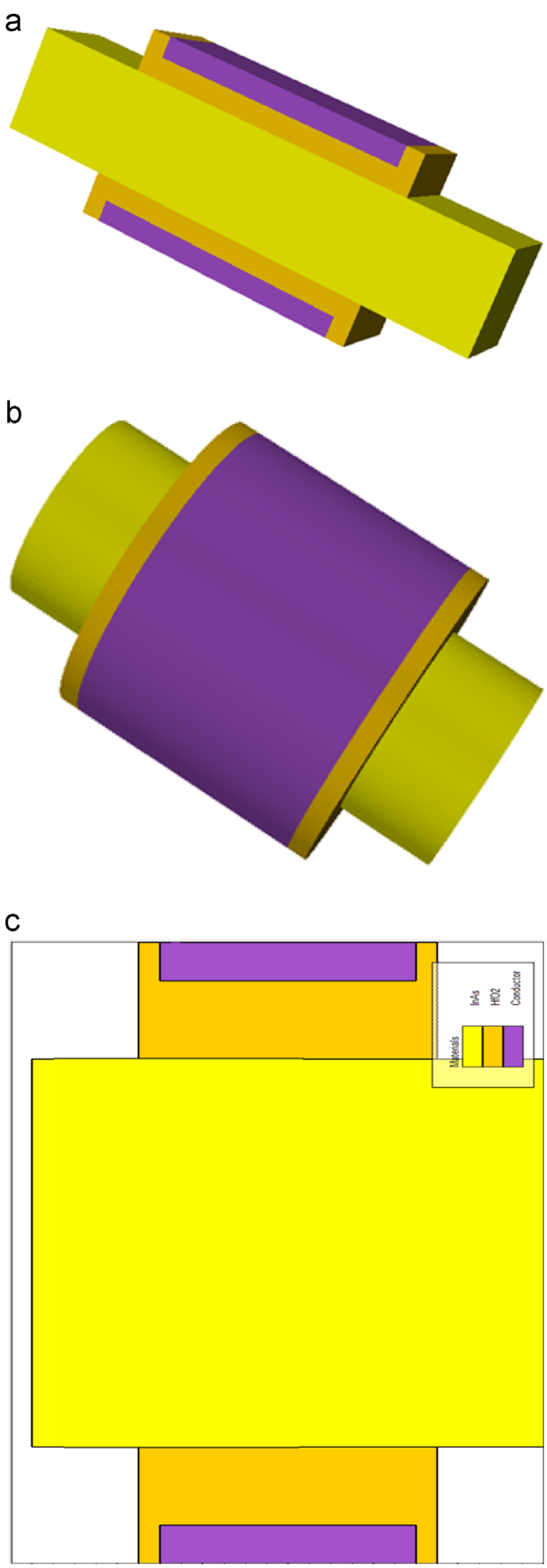


**Fig. 1.** (a) Schematic view of the Indium Arsenide (InAs) DG-MOSFET structure. (b) Schematic view of the Indium Arsenide (InAs) GAA-NWT structure. (c) Cross section view of the (a) and (b) structures simulated in this paper.

GAA and DG MOSFETs have emerged as promising devices to keep SCEs under control, exhibiting quasi-ideal sub-threshold slope with undoped channel. The use of a lightly doped or undoped channel maximizes the effective carrier mobility and hence ON current density. Also, the absence of dopant in the channel decreases the threshold voltage variations and drain to body capacitance which provide improved circuit performance [3].

At channel lengths under 15 nm the different reflections of SCEs are investigated by extraction of different parameters such as threshold voltage, sub-threshold slope, OFF-state current, and DIBL. Also, conventional classical models are not sufficient to describe the electrical characteristics of devices with channel lengths under 15 nm and the full quantum transport models need to be used for improved prediction of the device behavior [4,5].

For the first time in this paper, we present novel DG metal oxide semiconductor field effect transistor (MOSFET) and GAA nanowire metal oxide semiconductor field effect transistor (NWT) for diminishing the exchange-correlation (Ex-Corr). The key idea in this work is to use Indium Arsenide (InAs) semiconductor instead of Si. Mechanical transport approach based on the non-equilibrium Green's function (NEGF) method in consideration with Ex-Corr effect is employed. Our results demonstrate that the energy band-gap can be changed as the nanowire's diameter decreases and the nanowire's diameter can be changed by the material's character, e.g., from a direct to an indirect band-gap semiconductor or vice versa and ballistic transport (i.e. without scattering), can be occurred which can leads to markedly improved device performance. Also, the interaction between electrons and Ex-Corr effect is diminished in the proposed structure.

It is worth noting that quantum mechanical simulations in the ballistic limit have been carried out using the NEGF method previously [6,7]. But we would take into account Ex-Corr effect in this work.

## 2. Device parameters

The DG-MOSFET and GAA-NWT studied here are presented in Fig. 1. The parameters used for the devices in our simulations are summarized in Table 1.

Here we have incorporated high-k gate dielectrics such as Hafnium Oxide ($HfO_2$) to achieve better performance. We reduce the gate oxide thickness and the source/drain contact size that decreases the length by which the source/drain electric field penetrates into the channel, thereby, it improve the transistor characteristics and help to suppress the short channel effects. In the limit when the source/drain electrodes are reduced to wires with the same radius as the channel, the transistor can be well turned off and smaller contacts produce thinner Schottky barriers and improve the transistor performance [8].

**Table 1**
Parameters used for device simulation in this work.

| Parameter | GAA InAs NWT | DG InAs MOSFET |
|---|---|---|
| Channel doping | Undoped | Undoped |
| Source and drain doping | $10^{20}$ cm$^{-3}$ | $10^{20}$ cm$^{-3}$ |
| Channel length ($L_{ch}$) | 6 to 24 nm | 6 to 24 nm |
| Channel width | 5 nm | 5 nm |
| Oxide thickness ($T_{OX}$) | 2 nm | 2 nm |
| Gate workfunction | 6.35 eV | 6.35 eV |