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Room temperature quantum tunneling and Coulomb blockade in silicon-rich oxide

Zhenrui Yu [a,*], Mariano Aceves [a], Fuzhong Wang [b], Jesus Carrillo [c], Ragnar Kiebach [a], Karim Monfil [a]

[a] Department of Electronics, National Institute of Astrophysics, Optics and Electronics, Apdo. 51, Puebla, 72000 Pue., Mexico
[b] College of Science, Tianjin Polytechnical University, Tianjin, China
[c] CIDS-ICUAP, Universidad Autonoma de Puebla, Mexico

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ABSTRACT

We studied the electrical properties of silicon nanocrystals (Si-ncs) with a wide size distribution embedded in an oxide matrix. A wide Coulomb gap, clear current bumps, and significant current oscillations and jumps were observed at room temperature in the current vs. voltage characteristics of an Al/silicon-rich oxide/Si MOS-like structure. These anomalies can be well explained by quantum tunneling and Coulomb blockade effects. High-frequency capacitance vs. voltage, and conductance vs. voltage curves show jumps in similar voltage range supporting this explanation. The fact that the charging energy due to the Coulomb blockade effect is much larger than the quantum level spacing weakens the strict size-dependence of the quantum tunneling. The high density of Si-ncs in the oxide layer also enables the carriers to always find Si-ncs of similar size close enough to tunnel through.

1. Introduction

Self-assembly silicon nanocrystals (Si-ncs) embedded in dielectrics have drawn much attention from many researchers recently due to their potential applications in nanoelectronics and optoelectronics. Devices such as Si-based light-emitting diodes [1,2], single electron transistors [3], single electron memories [4], ultra-violet (UV) sensors [5] and photovoltaic solar cells [6] have been proposed. The electrical properties of Si-ncs are of particular importance for their applications. To date, the electrical properties of Si-ncs have been studied extensively [7–14]. A large diversity of experimental phenomena in electrical characterizations have been reported, such as single electron charge-trapping effect [7,8], resonant tunneling transport [9,10], current oscillations [11,12] and capacitance or current switches between different levels [13,14]. The reason for such a diversity of experimental observations may be due to the differences in the microstructure of the studied materials used in the course of the different studies. The density, shape, size and locations of Si-ncs in dielectrics should play an important role for their electrical properties. These parameters depend on the fabrication techniques and the deposition conditions, e.g., the excess Si content, substrate surface morphology, film thickness, etc. However, all above-reported results, which provide useful information for the deep understanding of the electrical properties of Si-ncs, can be associated with the quantum confinement and Coulomb blockade effect in the Si-ncs.

For carrier transport perpendicularly through an oxide layer consisting of Si-ncs, the Si-ncs play a key role. The embedded Si-ncs can form percolation paths for carrier transport, and hence the current is significantly increased. At low-electrical field, the carrier transport between Si-ncs is dominated by sequential tunneling, and other transport mechanisms such as Fowler–Nordheim tunneling can be neglected [15]. Thus the transport properties are very sensitive to the Si-ncs size, size distribution and their inter-distance (or the barrier thickness). It is generally believed that uniform Si-ncs are essential for observing quantum effects; thus, many experimental approaches trying to fabricate uniform Si-ncs have been devoted. However, synthesis of uniform Si-ncs embedded in a dielectric is not an easy work although a success has been achieved by using a superlattice approach [16]. On the other hand, our recent experimental results indicate that significant quantum effect can still be observed in a self-assembled Si-ncs/SiO_2 system with large variation in Si-ncs sizes [11]. One possible reason for our samples is that the charging energy due to the Coulomb blockade effect is much larger than

* Corresponding author. Tel.: +52 222 2663100x8222; fax: +52 222 2470517.
E-mail addresses: yinaoep@yahoo.com, zyu@inaoep.mx (Z. Yu).

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quantum level spacing, thus weakening the sensitive size-dependence of the quantum tunneling [9]. Another reason could be due to the high density of Si-ncs in oxide, which was achieved by controlling both the partial pressure ratio of the reactant gases and the substrate surface texturing.

In this article, we report significant resonant tunneling and current oscillations in an Al/silicon-rich oxide (SRO)/Si metal-oxide-semiconductor (MOS)-like structure. The SRO layer is a two-phase material with high density of Si-ncs embedded in an oxide matrix fabricated by low-pressure chemical vapor deposition (LPCVD) method. The results indicate that significant room temperature resonant tunneling and Coulomb blockade effects can be observed in a "large device" with random distributed self-assembly Si-ncs. These results are of significance in future devices made of self-assembly nanocrystalline silicon based on resonant tunneling and Coulomb blockade effects.

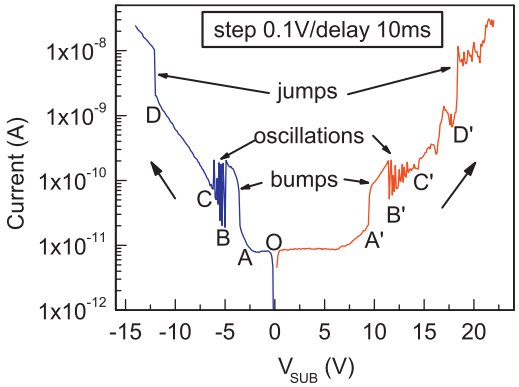

Fig. 1. Typical *I–V* curves under surface accumulation and inversion conditions. The voltage sweep directions are indicated by arrows.

2. Experiments

The samples have an Al/SRO/Si MOS-like structure, where the SRO layer is a two-phase material consisting of Si-ncs embedded in an oxide matrix. The SRO layer with a thickness of ~600 nm was deposited by LPCVD on n-type c-Si wafers with a (1 0 0) orientation and a resistivity of ~1–3 Ω-cm. The surface of the c-Si substrates was mechanically polished with 1-μm diamond sand, producing a high density of scratches and pits. The reason for the substrate surface texturing is to obtain a high density of Si-ncs in the deposited layer because the pits and scratches may act as nucleation sites. Standard RCA (Radio Corporation of America) cleaning process was performed on the substrates before putting them into the deposition chamber. The SRO layer was deposited at 725 °C with SiH_4 and N_2O as reactant gases. The partial pressure ratio Ro, which is defined as $Ro = P(N_2O)/P(SiH_4)$ was fixed to 10 during the deposition. After depositions, the films were thermally annealed at 1100 °C in N_2 for 3 h to crystallize the Si-ncs. The microstructure of the SRO layer was studied using a transmission electron microscope (TEM; Tecnai F30, PHI company) operated with an acceleration voltage of 300 kV. Front Al gate electrodes (area $A = 9.5 \times 10^{-3}\,cm^{-2}$) were evaporated on the annealed samples and back-contacts were also made by evaporating Al after etching off the native oxide layer. Dark quasi-static current vs. voltage (*I–V*) characteristics were measured using a computer-controlled Keithley 6517 electrometers. The applied voltage was swept step-by-step with variable sweep speed by changing the step voltages and delay times. High-frequency (110 kHz) capacitance vs. voltage (*C–V*), and conductance vs. voltage (*G–V*) characteristics were measured using a Keithley 590 CV analyzer. All measurements were performed at room temperature in dark with the bias voltage applied to the substrate (V_{SUB}).

3. Results

Fig. 1 shows the typical *I–V* curve of the devices. Clearly, in both bias directions similar anomalies were observed. At small bias voltages (OA, OA′), there is only a very small leakage current. At points A and A′, the current rapidly increased to high level, and this high current was kept for a period of voltage (regions AB and A′B′). The threshold voltages for the rapid current increase are $V_A = 1.75$ and 6.12 V, for negative and positive substrate biases, respectively. At points B and B′, the current jumps to a low value, forming current bumps (regions AB and A′B′) followed by random oscillations (regions BC and B′C′), the oscillations terminate at points C and C′. After that, the current smoothly increases till points D and D′ where the current shows another jump to a higher level. Sometimes, the current still shows some switches in different current levels when $V > V_D$ as shown in Fig. 1. The anomalies appear at different voltages for positive and negative biases possibly due to the asymmetric MOS-like device structure of the studied devices. When the n-type Si substrate was positively biased, it would exhaust some part of applied voltage and thus the current anomalies appeared at a larger value of voltage compared to the opposite bias direction as shown in Fig. 1.

Fig. 2 (A) and (B) shows *I–V* curves of the devices measured using different delay times and sweep directions, respectively. From Fig. 2(A), one can find that the leakage current in the voltage range of (0 to −2 V) depends on the delay time. Slower voltage sweeps produce smaller leakage current. In the case of step delay time of 3 s, the current approaches the lowest limit of the measurement system. This result indicates the leakage current is a displacement current produced by the charging of the stray capacitance of the device and measurement system, and will not be considered in the next. In this case, the drift current through the SRO layer in the voltage range of (−2 to 8 V) is zero and a wide Coulomb gap (AA′) was thus observed in Fig. 1. Another feature shown in Fig. 2(A) is that the current bump is almost independent of the step delay time. This indicates the current bump is produced by static transport of carriers through the SRO layer and some special conduction mechanisms are set up in this voltage range. However, the current oscillations in region BC depend on the step delay time. At very slow voltage sweep (step delay time 3 s), the oscillations disappear. Fig. 2(B) shows that the current jump at point D depends on the charge-trapping conditions and thus the charging history of the SRO layer. If the SRO layer traps more charges, point D moves to lower voltage. When the voltage sweeps from a large magnitude to a small one, point D appears at lower voltage because in this case more charges have been trapped in the SRO layer. Fig. 2(B) also indicates that the current bump and oscillations do not depend on the voltage sweep directions and this again confirms that they are ascribed to the carrier transport through the SRO layer via a kind of special conduction channel. This will be discussed later.

Fig. 3 shows the high-frequency *C–V* and *G–V* curves. In the voltage region where current bump and oscillations were observed (region AC), some anomalies also appear in *C–V* and *G–V* curves. The capacitance and conductance show some very regular jumps among different levels. The positions of these jumps are random, however, similar jumps were always observed in repeated measurements and in most of the devices of the wafer.