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Single-electron logic based on capacitively coupled double quantum dots

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Abstract

We propose a new single-electron logic based on a capacitively coupled double quantum dot structure. The structure could be viewed as a pair of single-gated single-electron transistors (SET) with their "islands" capacitively coupled to each other. The numerical modeling, based on an orthodox Coulomb blockade theory, shows the unique transport characteristics of the capacitively coupled system. By choosing the two gate voltages as input states and the source–drain current magnitudes as output states, specific logic functions (NAND and exclusive-NOR) can be implemented. It shows that this new logic not only inherits the advantages of the SET-based logic circuits, but also greatly reduces the element-per-function for the implementation of logic functions.

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Keywords: Single-electron logic; Quantum dot; Coulomb blockade; Capacitive coupling

1. Introduction

The last decade witnessed more and more experimental and theoretical efforts devoted to realizing the next generation single electron logic devices [1–11]. Generally speaking, these approaches can be categorized into two major types, one is the charge-state logic, represented by the quantum cellular automata (QCA) [2,3,8–9] and the binary decision diagram (BDD) logic [2,3,10–11]; the other one is the voltage-state logic based on the single-electron transistors (SET) [2–7]. Though the charge-state logic boasts the "ultimate single electron device" in a sense that it uses only one elementary charge for the bit-representation, the SET-based logic enjoys inherent advantages from the full-fledged CMOS techniques and thus is expected to be one of the most promising candidates for realistic large-scale integrated logic in the near future [2,3].

By simply using a single-gated configuration SET as a replacement for the conventional CMOS transistor, as proposed by Chen et al. [4], a functionally complete logic set could be implemented. However, the element-per-function for the logic function is still the same as their CMOS logic counterparts, due to the borrowed "architecture" from the conventional CMOS devices [2,3]. On the other hand, the multi-gated SET configuration, where more than one gates are capacitively coupled to one SET "island", provides the chance to linearly combine (i.e. summation, $\sum_i V_{g,i}C_{g,i}$) the input signals (gate voltage states) to influence the number of electrons in the "island" (or modulate the transport current) to implement specific logic functions. On the basis of this scheme, the element-per-function of some logic functions can be greatly reduced [2,3,5]. For instance, Takahashi et al. [5] report the experimentally implementation of XNOR function on a top silicon (Si) layer of a Si-on-insulator (SOI) wafer by using pattern-dependent oxidation technique. Also, an exclusive-NNOR operation by using a highly doped SET is presented by Kitade and Nakajima [6]. Moreover, a high-level logic function of "decimal adder" has also been proposed by Fahmy and Ismail [7] in a single two-gated SET configuration.

In addition to the extensively investigated tunneling coupling [12–15], the interdot capacitive coupling can also

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effectively correlate the charging and transport properties in the double dots, and thus provide another important basis for implementing new logic functions [16–20]. Previously, Hofmann et al. [16] investigated the shifting of conducting state of quantum dot (from conduction maximum to Coulomb blockade minimum) due to the addition of a single electron in a nonconducting neighbor dot via interdot capacitive coupling. Orlov et al. [17] reports the correlated motion of electrons in capacitively coupled metal double dots, where charging state of one double dot controls the tunneling rate through the other double dot . More recently, strong capacitively coupled double dot system (with negligible interdot tunneling coupling), in a two dimensional electron gas (2DEG) in GaAs/AlGaAs heterostructure, has been reported by Chan et al. [19]. By using unique trench isolating and "metal gate bridging" techniques, strong edge-on interdot capacitance can be achieved, and the transport properties through the nonlinear conductance versus charge behavior can be utilized to implement single-electron switch [20]. However, the application potential of the capacitively coupled double dot structure has not yet been fulfilled.

In this letter, we propose a single-electron logic based on a capacitively coupled double quantum dot structure. As shown in Fig. 1, the structure consists of two quantum dots arranged in parallel and connected to two electrodes by two pairs of tunnel barriers. It could also be viewed as a pair of single-gated SETs with their "islands" capacitively coupled to each other.

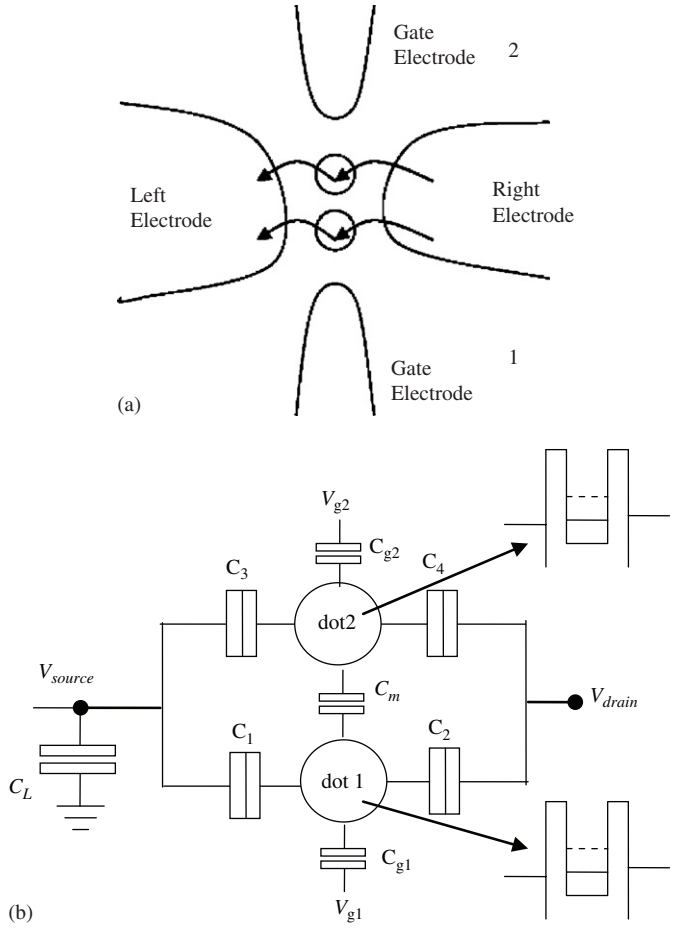

Fig. 1. (a) Schematic diagram for the capacitively coupled double dot structure and (b) the equivalent circuit for the structure.

As shown in our numerical modeling, the capacitive interdot coupling effectively correlates the states of the two dots and gives rise to unique transport characteristics of the double dot system. By virtue of this correlated feature, specific logic (like NAND and EXNOR) can be directly implemented, while the corresponding element-per-function can be greatly reduced in comparison with their counterpart in conventional CMOS architectural and previously proposed SET-based logic [4].

2. Formulation of the problem

We start with the introduction of the theoretical basis of the simulation model. As shown in Fig. 1a, the proposed structure composes a pair of capacitively coupled identical semiconductor quantum dots, connected to the left (drain) and right (source) electron electrodes via two pairs of tunneling barriers. The equivalent circuit is shown in Fig. 1b, where the interdot Coulomb interaction between the two dots is represented by an interdot capacitance C_m between the two dots [15,21]. The tunnel junction capacitances (C_t with $t = 1, 2, 3, 4$) and the two gate capacitances C_{g1} and C_{g2} are labeled as shown in Fig. 1b. The inset of Fig. 1b shows the energy diagram for each dot. For analytical clarity in this model, all the energy parameters are normalized by the single dot Coulomb blockade energy $U = e^2/C_{dot}$. As a matter of convenience, we consider only the ground quantum confinement state (two-fold spin degeneracy) in each dot.

In a sequential tunneling limit, the tunnel rate width of the discrete level is assumed to be much less than the characteristic energy scales of each dot. Thus, the occupation numbers of the quantum dots are still good quantum numbers and a master-rate-equation approach can readily be adopted to describe the transport through the capacitively coupled double dot structure [1,22].

The states of the double dot system are formally defined in an occupation notation $\{n_1, n_2\}$, where n_1 (n_2) denotes the number of electrons in the dot1 (dot2) and could take on only the values of 0, 1 and 2. And the electrostatic energy for the coupled double dot system, consisting of the intradot Coulomb blockade energy and the interdot Coulomb interaction energy, as well as the part subjected to the influence of two gate voltages, reads

$$E_{n_1,n_2} = \sum_{i=1}^{2} \frac{e^2 n_i^2}{2C^*_{\sum,i}} + \sum_{\substack{i,j=1 \\ i\neq j}}^{2} \frac{e^2 n_i n_j}{C^*_m} - \sum_{i=1}^{2} e n_i \alpha_i V_{g,i}, \quad (1)$$

$$C^*_{\sum,1} = C_{\sum,1}\left(1 - \frac{C_m^2}{C_{\sum,1} C_{\sum,2}}\right),$$