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Demonstration of gating action in atomically controlled Si:P nanodots defined by scanning probe microscopy

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Abstract

We study the low temperature electrical characteristics of planar, highly phosphorus-doped nanodots. The dots are defined by lithographically patterning an atomically flat, hydrogenated Si(1 0 0):H surface using a scanning-tunneling-microscope (STM), phosphorus δ-doping and low temperature molecular beam epitaxy in an ultra-high vacuum environment. Ohmic contacts and a surface gate structure are aligned *ex-situ* using electron beam lithography. We present electrical transport measurements of a $25 \times 21\,nm^2$ Si:P nanodot at 4 K containing about 1000 P atoms. We find significant gating action within a gate range of -2 to 7 V. From the stability diagram, we observe a large conductance gap and the existence of electron resonances near threshold which can be modulated with the top gate. Our results show promise for the fabrication of planar quantum dots using this technique.
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1. Introduction

Single electron charging phenomena [1] in solid state systems have been studied extensively over the last two decades opening up a new field of research. Quantum dots electrostatically defined by confinement of a two dimensional electron gas (2DEG) in GaAs have been the most commonly studied solid state quantum dot system but within the past two years reliable gating [2] of 2DEGs formed by Si/SiGe heterostructures has become possible. This has allowed the investigation of electron transport through quantum dots in silicon [3].

In this paper we show how planar, ultra-dense Si:P nanodots can be realized using a novel fabrication strategy [4,5] based on STM lithography, local P δ-doping and low temperature Si molecular beam epitaxy. In particular, we demonstrate gating of a $25 \times 21\,nm^2$ Si:P dot containing about 1000 P atoms. Conductance measurements at 4 K reveal a large conductance gap reminiscent of Coulomb blockade and the presence of several electron resonances superimposed on a rising conductance background.

2. Device fabrication

For the fabrication of highly planar devices, we have developed a silicon step engineering process in which dopants are patterned by scanning probe lithography onto one atomic plane of the silicon surface. This is achieved by wet chemically pre-patterning the silicon substrate, which then rearranges during the high temperature anneal required to prepare atomically flat surfaces in ultra-high vacuum (UHV). Previously, optical lithography was used to define etched registration markers [6] in the silicon substrate approximately 5.5 μm away from the active device region. After the high temperature anneal required to achieve the Si(1 0 0) 2×1 surface reconstruction, we

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found that the active device area consisted of atomically stepped terraces but were unaffected by the presence of the markers which were located far away. We have recently transferred this process to the use of electron beam lithography (EBL) which allows the patterning of smaller marker features [7,8], thereby allowing higher resolution alignment of surface features once removed from UHV. After subsequent etching of the Si(1 0 0) surface using tetra-methyl-ammonium-hydroxide as an etching agent, we now find, that we can achieve an atomically flat surface in the device region after etching four markers arranged in the corners of a $2.5 \times 2.5\,\mu m^2$ square, see Fig. 1(a). After the surface is annealed to $1200\,^{\circ}C$ for 10 s, the proximity of the markers induces the formation of a monoatomic, circular terrace with a diameter of up $\sim 1\,\mu m$. This is an ideal starting surface for the patterning of the active device region on a single terrace. Fig. 1 also shows an example of

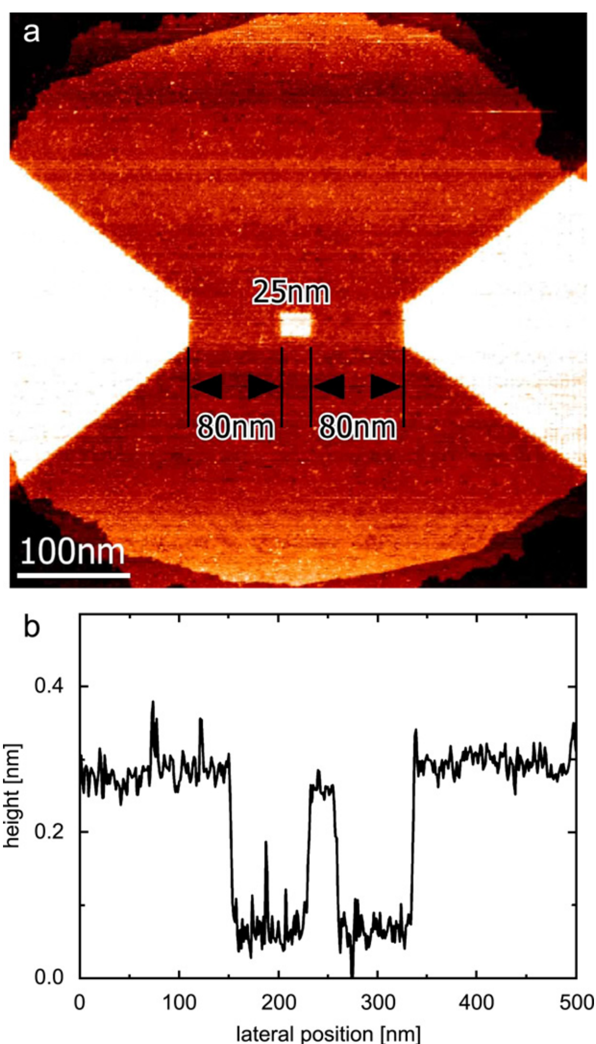

Fig. 1. (a) STM image of a lithographically defined nanodot with source-drain leads patterned on a single Si(1 0 0):H terrace, (b) a line profile showing an atomically flat surface. The apparent height increase in the lithographic dot structure is due to dangling electron bonds from the underlying silicon dimers. These are highly reactive to the molecular chemisorption of PH_3 used as the dopant source.

a Si:P nanodot patterned by STM lithography on a hydrogen terminated Si(1 0 0):H surface, where the white areas correspond to regions where the hydrogen has been desorbed by the STM tip, revealing source drain contacts with a 25 nm dot. Note that in the horizontal line profile across the dot shown in Fig. 1(b), the apparent height change within the lithographic region is electronic in nature and due to the additional tunneling current from the silicon surface states of the underlying Si dimers in the dot and source-drain regions [9].

We have recently pursued another method to realize large, step-free terraces by patterning micron-sized inner circular markers [7] which allows the formation of a monoatomic plateau in its center thus providing extra alignment capability. In the following, we describe how the circular marker technique has been used to fabricate a top-gated $25 \times 21\,nm^2$ Si:P dot with source-drain leads. After the formation of etched registration markers for device positioning and relocation on a $1 \times 1\,cm^2$ large, Si(1 0 0) sample (n-type with a resistivity of $1-10\,\Omega\,cm$), it is introduced into the UHV environment. After a sample anneal to $1200\,^{\circ}C$ for 10 s to form the 2×1 surface reconstruction and hydrogen resist formation, we pattern the device structure into the monohydride resist using STM lithography. Fig. 2(a) shows an STM image of the $25 \times 21\,nm^2$ dot pattern with adjacent source-drain leads and separations of 21 and 23 nm, respectively. Note that on either side of the source-drain contacts shown, two $800 \times 800\,nm^2$ sized regions were also desorbed using STM lithography. These serve to act as contact regions to subsequent surface leads as described below.

P dopant incorporation into the Si top layer is achieved by molecular chemisorption of PH_3 and subsequent P incorporation mediated by a thermal anneal at $350\,^{\circ}C$ [10]. The device chip is then encapsulated with 25 nm of epitaxial silicon using low temperature molecular beam epitaxy at $250\,^{\circ}C$ [11] followed by growth of a 50 nm-thick room-temperature SiO_2 barrier using a novel UHV-compatible technique employing an atomic oxygen source [12].

The sample is then taken out of UHV and electron beam lithography is used to align two surface contacts to the buried, STM-patterned doped source-drain leads using the etched markers [7]. Note that the SiO_2 is etched away in a buffered hydrofluoric acid bath around the terminals before Al is evaporated to form metal leads which vertically overlap with the two P-doped $800 \times 800\,nm^2$ regions connected to the source-drain of the buried Si:P dot. Ohmic contact to the buried device is achieved after annealing the surface aluminium at $350\,^{\circ}C$ in a nitrogen atmosphere. In a further EBL step, a 164 nm wide surface gate is aligned on top of the buried dot structure, in between the source-drain metal contacts with a separation of 159 and 164 nm, respectively. Fig. 2(b) shows an SEM image of two contact terminals and the top gate across the center of the device with an absolute alignment accuracy to the buried dot below 100 nm. Using atomic force microscopy, we can confirm that the SiO_2 has been entirely

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