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Electrical and memory properties of silicon nitride structures with embedded Si nanocrystals

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Abstract

In this work, the electrical and memory behaviour of metal-silicon nitride-silicon structures with an embedded nanocrystalline silicon layer, which either consists of separated silicon nanocrystals, or is a continuous nanocrystalline layer, are presented. The structures were prepared by low-pressure chemical vapour deposition (LPCVD). The effect of the duration of deposition and the structure of the nanocrystalline layer were studied. The writing/erasing behaviour was similar for all the structures, but the retention properties were much worse in the structure with a continuous nanocrystalline layer, than in the structures with separated Si nanocrystals. This indicates that Si nanocrystals play role in charge storage in the studied structures.

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1. Introduction

Dielectric layers with embedded semiconductor nanocrystals have been widely studied recently in order to overcome difficulties of non-volatile memory devices connected with technology scale down [1–9]. The main problem with scaling down of floating gate memory transistors is that the required thin tunnel oxide layers of 2–4 nm are not reliable enough [10]. In the case of the presence of any defect, the whole stored charge will leak through the defect area. However, if separated Si nanocrystals (nc-s) are used as charge storage media, the stored information will not be lost.

Now a days, both the tunnel and control dielectric layers in memory FETs and arrays are usually SiO_2 layers. However, Si_3N_4 can also be used for control layer, as in the case of well-known MNOS devices, which were the first realised memory structures. Si_3N_4 control layer has the advantage above SiO_2 of a higher dielectric constant, yielding higher electric field in the tunnel oxide for the same layer thicknesses and voltage pulses.

Si nc-s can be formed in Si-rich SiN_x layers by different CVD deposition techniques even without postdeposition annealing [11–13]. However, in this case, Si nc-s are distributed along the whole layer, while memory structures require a thin nc layer just near the tunnel oxide.

In this work, our goal has been to create such memory structures with a thin nc layer by low-pressure chemical vapour deposition (LPCVD). To study the effect of deposition parameters on the thickness and microstructure of nc-Si layer, SiN_x/nc-Si/SiN_x structures were grown at different conditions [14]. In this paper, the electrical and memory behaviour of a series of Si_3N_4/nc-Si/Si_3N_4 structures exhibiting good memory behaviour are briefly summarised.

2. Experimental

In the reported series of Si_3N_4/nc-Si/Si_3N_4 structures, the effect of the deposition time of the middle nc-Si layer was studied. All the layers were deposited by LPCVD on n-type Si substrates at 830 °C at a pressure of 30 Pa using SiH_2Cl_2 and NH_3 in three steps. The content of the top and bottom layers of the structures was stochiometric Si_3N_4. The

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stochiometric layers were grown at gas flow rates of SiH_2Cl_2 and NH_3, respectively of 21 and 90 sccm, while the middle nc-Si layer was grown with a gas flow rate of SiH_2Cl_2 of 100 sccm. The duration of deposition for the nc-Si layer varied from 30 to 120 s. The duration of the deposition and the thickness of the layers are summarised in Table 1. A reference structure without any nc-Si layer was also prepared with a Si_3N_4 layer thickness of 40 nm (Sample NI000). For electrical and memory measurements, Al capacitors were formed with dimensions of 0.8 mm × 0.8 mm by evaporation. For the back-side ohmic contact also, Al was used after an appropriate chemical surface treatment using a mixture of H_2SO_4 and H_2O_2 [15].

The thickness and microstructure of the layers were studied by high-resolution cross-sectional transmission electron microscopy (HRTEM). Current–voltage (I–V), capacitance–voltage, memory hysteresis, memory window, and retention measurements were performed at room temperature.

3. Results and discussion

HRTEM measurements indicated that shorter durations yielded nc-Si layers with separated nc-s, while for the structure prepared with the longest duration of 120 s, a continuous nc-Si layer was obtained, as presented in Fig. 1 for structures NI060 and NI120.

The current flow through the structures at high current levels was dominated by the Poole–Frenkel mechanism, which can be expressed as

$$J_{PF} = C_{PF1} E \exp(C_{PF2}\sqrt{E}). \quad (1)$$

The fit of this expression yielded parameters of $C_{PF1} = 8.0 \times 10^{-26}\,A\,V^{-1}\,m^{-1}$ and $C_{PF2} = 1.48 \times 10^{-3}\,V^{-1/2}\,m^{1/2}$. The agreement between the experimental and fitted by Eq. (1) theoretical curves is shown in Fig. 2 for the structure NI060 prepared with duration of 60 s. However, an exponential excess current was also obtained at low current levels (see Fig. 2), which can be expressed as

$$J = C_{EX1} \exp(C_{EX2} E) \quad (2)$$

with parameters of $C_{ex1} = 1.5 \times 10^{-7}\,A\,m^{-2}$ and $C_{ex2} = 1.55 \times 10^{-8}\,V\,m^{-1}$.

The good memory behaviour obtained for structures with Si nc-s are demonstrated in Figs. 3–5. Fig. 3 presents the memory hysteresis (the dependence of the flat-band voltage on the amplitude of charging–recharging voltage pulses, when the amplitude is gradually increased and then decreased) for the structure NI060 prepared with duration of 60 s, while Fig. 4 presents the memory window width for the same structure obtained for charging/erasing pulse duration of 400 ms, as a function of the pulse amplitude. The required high amplitudes are necessary because of the thick layers used in the studied structures.

All the structures exhibited similar memory hysteresis and memory window behaviour. The memory window width for the different structures is summarised in Table 2 for pulse amplitude of ±20 V with duration of 400 ms.

But a significant difference was obtained between the retention behaviour of the structures with separated Si nc-s or without nc-Si layer (structures with duration of 0–60 s, NI000–NI060) and of the structure with a continuous nc-Si layer (structure with duration of 120 s, structure NI120). The change of the memory window as a function of time after application of charging/erasing pulses with amplitude of ±20 V and duration of 400 ms is shown in Fig. 5 for structures NI060 and NI120. The retention rate depended on waiting time in all samples. A fast charge loss was obtained after switching off the charging pulse, which gradually converged to a lower value. The structure with a continuous nc-Si layer exhibited much faster loss of the stored charge, as it is seen in Fig. 5. The retention rate for injected holes and injected electrons was the same in the structure with a continuous nc-Si layer (0.81 V/decade), but it was higher for holes (0.60 V/decade), than for electrons (0.39 V/decade) in the structure with Si nc-s. This observation is just opposite to that published recently for Si nc-s embedded in SiO_2 [6]. The difference must be connected with the different band structure of Si_3N_4 and SiO_2.

The normalised rate of memory loss (the rate of the decrease in memory window width divided by its initial value) obtained after convergence of the retention rate to a constant value and the extrapolated value of the memory window width after 1 year are also presented in Table 2 for all the studied structures. The normalised rate of memory loss is in the range of 0.072–0.082 per decade for structures with Si nc-s and the reference sample, while it is higher by a factor of about 1.6 for the structure with a continuous

Table 1
Deposition times and layer thicknesses extracted from XTEM images for the examined Si_3N_4/nc-Si/Si_3N_4 structures

	Sample NI030		Sample NI045		Sample NI060		Sample NI120	
	Deposition time (s)	Thickness (nm)	Deposition time (s)	Thickness (nm)	Deposition time (s)	Thickness (nm)	Deposition time (s)	Thickness (nm)
Top Si_3N_4 layer	600	32	600	32	600	31	600	33
Middle nc-Si layer	30	2	45	5	60	7	120	13
Bottom Si_3N_4 layer	300	14	300	15	300	15	300	16