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Solar Energy 107 (2014) 489–494

SOLAR ENERGY

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# Fabrication of novel hybrid antireflection structures for solar cells

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Received 29 January 2014; accepted 4 May 2014
Available online 28 June 2014

Communicated by: Associate Editor Dr. Takhir Razykov

**Abstract**

In solar cell technology, surface texturing is essential for reducing the reflectance of cell surfaces and increasing their efficiency. This study employs photo-assisted electrochemical etching (PAECE) to fabricate a hybrid structure comprising a reversed pyramid structure and a high aspect ratio macro-pore on the silicon wafer surface, to reduce cell surface reflectance. The experimental results show that the etching depth of the fabricated macro-pore array structure was approximately 67.1 μm and its diameter was approximately 5 μm on the 525-μm-thick sample, such that the aspect ratio of the pore was approximately 13.4:1. The mean reflectance of a blank silicon wafer is 37.4% in the wavelength range of 280–800 nm; however, the reversed pyramid created using a 120-min PAECE process and 25-min RIE can reduce the mean reflectance to 0.7% on the 380-μm-thick sample. The novel fabrication process developed in this study is low cost and the hybrid structure can be applied to antireflection structures in single crystalline silicon solar cells.
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*Keywords:* SANSL; Antireflection structure; Solar cell

## 1. Introduction

In recent decades, numerous researchers have studied the surface texture of silicon wafers (Vazsonyi et al., 1999; Zhao et al., 1999; Menna et al., 1995; Tsakalakos et al., 2007; Lee et al., 2008; Huang et al., 2007). These studies have sought to produce micro- or nano-scaled structures on a substrate, reducing the reflectance from silicon wafers and increasing the efficiency of solar cells. Moreover, textured structures possess more surface area compared with a planar surface and increase the possibility of receiving photons from incident light (Fig. 1). Texturing approaches include random pyramids (Vazsonyi et al., 1999), inversed pyramid arrays defined using photolithography (Zhao et al., 1999), porous silicon structures generated using electrochemical etching (Menna et al., 1995), and subwavelength structures (SWS) (Tsakalakos et al., 2007) in which the structure width is smaller than the wavelength of light and the structure has a periodic arrangement. In micro-scaled antireflection structures, the increased surface area is insufficient compared with the nano-structure, and its chances of reflecting incident light are also less compared with nano-scaled structures (Fig. 1b and c). By contrast, the *P–N* junction region formed in nano-scaled structures cannot be as large as the surface area because of the narrow space between the structures. As shown in Fig. 1(c), when the cell surface was modified to *P*-type, forming a *P–N* junction in an

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http://dx.doi.org/10.1016/j.solener.2014.05.009
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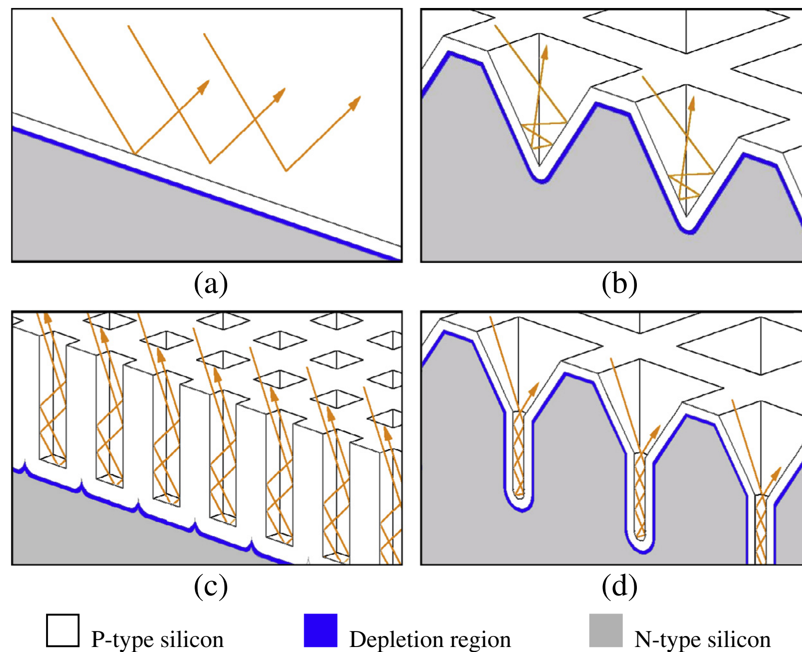


Fig. 1. Schematic diagram of light reflection and *P–N* junction formation on the (a) planar surface; (b) micro-inverted pyramid; (c) nano-scaled structure; and (d) hybrid structure developed in the current study.

*N*-type solar cell comprising a nano-structure, the entire nano-structure region became a *P*-type material. Thus, the nano-scaled structure effectively increases the reaction area but is not guaranteed to enlarge the *P–N* junction region.

In the current study, a novel antireflection structure is presented, improving the inversed pyramid structure using the photo-assisted electrochemical etching (PAECE) technique. The PAECE technique is a well-known and low-cost etching approach (Uhlir, 1956; Turner, 1958; Lehmann, 1995; Lehmann and Grüning, 1997; Lehmann and Föll, 1990) that creates aspect ratios in etched structures as high as 250:1 (Lehmann, 1995). The PAECE process was adopted to generate a high aspect ratio hole from the tip of a micro-scaled inversed pyramid. Researchers hypothesized that this novel structure possessed a large reflective surface area. Moreover, because the space between the high aspect ratio holes is micro-scale, the *P–N* junction region area could close to surface area, as shown in Fig. 1(d).

## 2. Experimental design

Fig. 2 shows the flow chart for fabricating a hybrid structure on a silicon substrate. This study employed a 4-inch *N*-type silicon wafer; its resistance was 1–100 Ω cm and its thickness was 525 μm. Low pressure chemical vapor deposition was used to deposit 400 nm of silicon nitride onto the wafer surface, creating an etching mask for the PAECE process. To fabricate a 380 μm-thick silicon substrate, the back side nitride layer of a 525 μm-thick wafer was first removed using an RIE (reactive ion etching) process and $CF_4$ plasma. Potassium hydroxide (KOH) was then employed to etch the backside of the wafer until the appropriate thickness was reached.

The PAECE etching patterns in the mask were arrayed in a square of 40 μm × 40 μm, at a pitch of 10 μm. A lithography process using an S1813 photoresist and an RIE process was applied to define the etching window of a silicon nitride layer. The inverted pyramid structure was obtained using KOH, and a conductive layer of Cr/Au (2 nm/20 nm) was then coated on the backside of the silicon using the PAECE process, such that the etching bias could be uniformly distributed on the sample. Fig. 3 shows the experimental scheme of the PAECE technique. The distance between the platinum cathode and the anodic sample was 3 cm, and a 340 W xenon lamp was applied to irradiate the backside of the sample during the PAECE process. An electrolyte was prepared using DI water, ethanol, and hydrogen fluoride (HF) at a volume ratio of 14:5:1. The substrates were 380 μm and 525 μm thick and the etching time ranged from 30 min to 120 min. The PAECE process was operated at a temperature of 22 ± 1 °C and no agitation was used during the etching experiment. Scanning electron microscopes (SEM; JEOL JSM-6360) were employed to observe the morphology generated by each process and a spectrometer (Perkin Elmer Lambda 900) was used to evaluate the relationship between the etching time and the reflectance of the sample.

## 3. Experimental results

### 3.1. Fabrication of the macro-pore array structure

Figs. 4 and 5 indicate that the macro-pore array structures were obtained using KOH and PAECE to etch at

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