Superlattices and Microstructures 98 (2016) 37–45

Contents lists available at ScienceDirect

Superlattices and Microstructures

journal homepage: www.elsevier.com/locate/superlattices

Investigating the performance of SiGe embedded dual source p-FinFET architecture

Kunal Sinha [a], Partha Sarathi Gupta [a], Sanatan Chattopadhyay [b], Hafizur Rahaman [a, *]

[a] School of VLSI Technology, Indian Institute of Engineering Science and Technology, Shibpur, Howrah, 711103, India
[b] Department of Electronic Science, University of Calcutta, 92, APC Road, Kolkata, 700009, India

ARTICLE INFO

Article history:
Received 27 June 2016
Received in revised form 3 August 2016
Accepted 7 August 2016
Available online 8 August 2016

Keywords:
SiGe
Dual-source
Bi-axial stress
p-FinFET

ABSTRACT

In this work, a modified Fin shaped Field Effect Transistor (FinFET) structure has been proposed with dual SiGe embedded extended source regions. Comparative simulation studies with SiGe embedded source/drain conventional single Fin channel and dual Fin channel FinFET structure having similar device footprint area shows almost 3× and 1.5× improvement of drive current respectively and lower threshold voltage in the proposed architecture. The dual extended SiGe source regions and presence of Si drain in the vertical direction of the channel generate bi-axial channel stress which improves the channel charge density, which results in improvement in drive current significantly. Also it has been observed from various simulation studies that the separated gate regions increase the inversion current density in the channel which also leads to improvement of the device performance.

1. Introduction

As the Field Effect Transistor (FET) channel length scaling enters sub-20 nm regime, the improved gate electrostatic control of multi-gate FET structures make them an attractive choice for advanced technology nodes device architectures [1,2]. The FinFET-based multi-gate (MuGFET) devices, has the advantage of reduced short channel effects (SCEs), leakage currents (I_{off}), threshold voltage (V_T) dopant fluctuations and possible higher mobility due to the un-doped channels [3–5]. Also, the main challenge for maintaining the performance improvement of Very Large Scale Integration (VLSI) circuits is the power consumption and to overcome it, the supply voltage scaling has been extensively used for the last 20 years [6–8]. On the other hand, carrier mobility improvement in the channel of FET devices, within the available VLSI process technologies, has been done by applying package strain technology, combination of new materials and different orientations in the channel [9]. However, the challenge of device performance improvement, within the supply voltage, fabrication cost and device geometry scaling constraint, has been conveniently overcome by the introduction of strain into the channel [10–14]. The strained channel improves the transport properties of the carriers due to reduction in conductivity effective mass and scattering [14,16]. When the drive current (I_{ON}) is increased by applying strain, it leads to reduction of carrier effective mass in the channel, resulting higher speed and performance for the same supply voltage in comparison to conventional Si architecture and thus the performance gain is achieved without changing the supply voltage and geometrical scaling [11,15].

* Corresponding author.
E-mail address: rahaman_h@yahoo.co.in (H. Rahaman).

http://dx.doi.org/10.1016/j.spmi.2016.08.004
0749-6036/

The initial works on strained-Si channel MOSFETs were focused on the substrate induced bi-axial stress where a virtual $Si_{1-x}Ge_x$ substrate was used to generate the stress in the Si channel region [12–15]. However, biaxial stress suffers from defects, Ge out-diffusion from the underlying $Si_{1-x}Ge_x$ substrate and performance loss at high vertical electric fields which lead to the degradation of interface quality of the device [14,15]. In contrast, the uni-axial strain in the channel, generated by embedded source/drain region, provides significantly large electron and hole mobility enhancement at both low strain and high vertical electric field in comparison to biaxial strain [11,16,17]. The uniaxial strain in the channel is applied by either SiGe embedded source/drain for p-channel device and by SiC embedded source/drain or Si_3N_4 capping layer on top of the n-channel device [10,18–20].

Several reports are available which show the differences and advantages of uniaxial stress over its biaxial nature for strained-Si [16], strained-Ge [21,22], and strained-SiGe [23] and SiGeSn [24] channel region. In this work, a modified p-FinFET structure (MOD-FinFET), having two extended SiGe embedded source regions and a single Si drain region, has been proposed where the strain technology has been used to improve device performance and split gate regions are used to keep the SCEs under control. The proposed structure has been designed using Sentaurus TCAD process and device simulator [26,27] and compared in terms of channel stress, and electrical performance parameters with SiGe embedded source/drain conventional FinFET architecture having similar dimensions. The effects of dimensional variations of source, channel and drain regions on the channel stress components and it's consequence on electrical characteristics and device parameters have also been studied.

2. Device design and simulation set up

The thermionic emission over the energy barrier is the key carrier injection mechanism in FET devices. In conventional p-FinFET structure, the holes injected into the channel from source region (p_S^+) is controlled by the following expression:

$$p_S^+ = \left(\frac{N_{2D}}{2}\right) f_S \tag{1}$$

where $f_S = \frac{1}{\left(1+exp\left[\frac{E_f - E_v}{KT}\right]\right)}$, and $N_{2D} = 2D\ density\ of\ state\ function.$

Similarly, the holes move to the drain region from channel (p_D^-) for the applied negative drain bias V_d and the charge transfer is controlled as,

$$p_D^- = \left(\frac{N_{2D}}{2}\right) f_D \tag{2}$$

where $f_D = \frac{1}{\left(1+exp\left[\frac{E_f - E_v + qV_d}{KT}\right]\right)}$,

Thus the total inversion charge transfer (Q_{inv}) through the channel becomes,

$$Q_{inv} = q\left[p_S^+ + p_D^-\right] \tag{3}$$

Now, from the concept of conventional MOSFET, it is well known that the total inversion charge can be expressed as [25],

$$Q_{inv} = C_{ox}\left[V_{gs} - V_{Th}\right] \tag{4}$$

where C_{ox} = gate oxide capacitance. V_{gs} = applied gate to source bias voltage. V_{Th} = threshold voltage.

The total gate charge balances the inversion charge. Thus following Eqns. (3) and (4),

$$q\left[p_S^+ + p_D^-\right] = C_{ox}\left[V_{gs} - V_{Th}\right] \tag{5}$$

Now, if the number of source terminal increases then the total amount of hole injection from source i.e. p_S^+ also increases which results to a reduction of threshold voltage for the same gate bias and oxide capacitance.

Thus, in case of dual source architecture, the total amount of hole injection from the source sides is,

$$p_{SA}^+ = \left(\frac{N_{2D}}{2}\right) f_{SA} \text{ and } p_{SB}^+ = \left(\frac{N_{2D}}{2}\right) f_{SB} \tag{6}$$

where $f_{SA} = f_{SB} = \frac{1}{\left(1+exp\left[\frac{E_f - E_v}{KT}\right]\right)}$, and $N_{2D} = 2D\ density\ of\ state\ function.$