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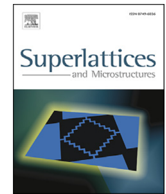

Study of strained-Si p-channel MOSFETs with HfO_2 gate dielectric

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In this work, the transconductance of strained-Si p-MOSFETs with high-K dielectric (HfO_2) as gate oxide, has been presented through simulation using the TCAD tool Silvaco-ATLAS. The results have been compared with a SiO_2/strained-Si p-MOSFET device. Peak transconductance enhancement factors of 2.97 and 2.73 has been obtained for strained-Si p-MOSFETs in comparison to bulk Si channel p-MOSFETs with SiO_2 and high-K dielectric respectively. This behavior is in good agreement with the reported experimental results. The transconductance of the strained-Si device at low temperatures has also been simulated. As expected, the mobility and hence the transconductance increases at lower temperatures due to reduced phonon scattering. However, the enhancements with high-K gate dielectric is less as compared to that with SiO_2.

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1. Introduction

In order to boost up the VLSI or ULSI circuits, new materials are being developed. The interest in advancement of growth of new material system is driven by the possibility of designing advanced electronic circuits by embedding the existing devices with a new material. Also device scaling is essential for performance improvement and to achieve high packing density in the ICs. But scaling of the gate oxide thickness results in increase of the unwanted gate leakage current in nano scale devices.

High-K dielectric is one of the promising candidates to address the roadblock to the thickness of SiO_2 gate oxide. But the scattering mechanisms and surface roughness at the interface of high-K gate oxide and Si degrades the surface carrier mobility. Hence for the mobility enhancement of the carriers, the conventional silicon surface can be replaced with biaxially tensile strained silicon on relaxed $Si_{1-x}Ge_x$ substrate which has the ability to increase both the hole and electron mobility. Hole mobility enhancement factor of 1.4 with 29% Ge with respect to that at 10% Ge content has been reported in literature [1]. Moreover, in some other literature the high-field hole mobility improvement at low temperature has been reported [2,3] with long channel strained-Si p-channel devices.

Thus the hole mobility enhancement with strained-Si channel and high-K gate oxide at low temperatures is an interesting area of research. In this paper, the proposed conventional 2-D structure of strained-Si p-MOSFET of gate length 0.5 μm (500 nm) has been simulated by TCAD suite from Silvaco and the device characteristics has been reported using ATLAS device

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simulator [4]. The mobility enhancement due to strain has been modelled using an analytic expression involving strain (Ge content) in the existing mobility model.

2. Device structure and simulation

The experimental results for the device fabricated by Rim et al. [1] are available for long and short channel devices, so a similar structure has been simulated as shown in Fig. 1. But in the following structure, the SiO_2 layer of 13 nm has been replaced by high-K dielectric HfO_2 of 73 nm thickness to maintain equivalent oxide layer thickness. In this structure, there is a strained and graded SiGe layer of 40 nm below the strained-Si channel to reduce the band offset between the strained-Si and SiGe substrate. This avoids the formation of a parasitic buried channel at the strained-Si/SiGe interface.

There is uniform boron doping of 1×10^{20} cm^{-3} in the source and drain of the device with n-type doping level of 6×10^{16} cm^{-3} in the bulk regions. The bulk layer interfaces are considered defect free but with a fixed oxide charge density of $5 \times 10^{10} cm^{-2}$. Simulation was done above 50 Å, so that quantum effect can be neglected.

For the device modelling and simulation, the material parameters of strained-Si and SiGe, like the band-offsets encountered in strained layers, the narrowing of band gap due to strain, band gap narrowing due to heavy doping and the mobility of carriers have been considered. The strained-Si energy band gap narrows down with respect to the silicon value following the relationship given in equation (1) [5]:

$$E_g = 1.08 - 0.4x \tag{1}$$

where, x is the value of Ge content in the top layer of relaxed SiGe.

Carrier mobility is the other important parameter for simulation. The introduction of strain affects the mobility through reduction in effective mass of carriers and also the intervalley scattering rate. The effect of strain has been implemented by modifying the doping, temperature and transverse field dependent mobility of Si given by Lombardi CVT et al. [6] with an analytic expression involving Ge content x [7] given by equation (2). Moreover, the effect of alloy scattering has been added with the modified CVT using Mathiessen's rule for the SiGe region [7].

$$\mu_{p,strained-Si} = \mu_{p,CVT}\left(1 + 4.31x - 2.28x^2\right) \tag{2}$$

The mobility due to alloy scattering in the SiGe region is given by:

$$\left[\mu_{alloy}\right]^{-1} = x(1-x)\exp(-7.68x)/124 \text{ for } x \le 0.2$$

and

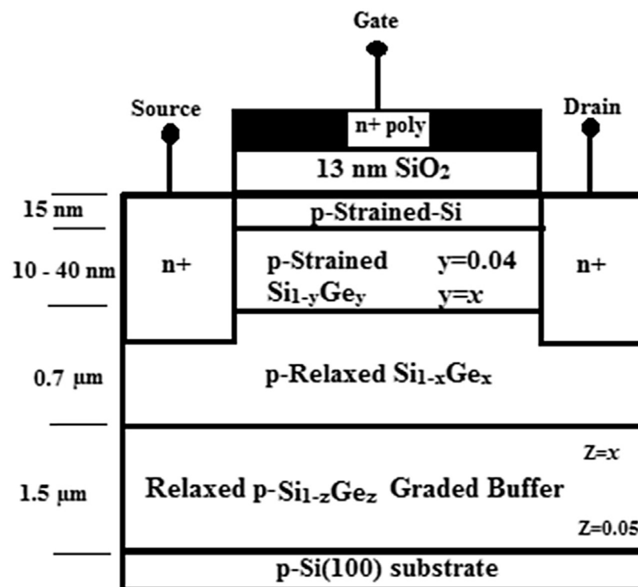

Fig. 1. Structure of a strained-Si p- MOSFET [1].

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