

Performance optimization of nanoscale junctionless transistors through varying device design parameters for ultra-low power logic applications

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ABSTRACT

Ultra-low power logic applications at advanced CMOS technology nodes have been extensively investigated nowadays to increase packing density in Integrated Circuits at a lower cost. Junctionless (JL) transistors have emerged as promising alternatives to conventional MOSFETs because of their relatively easy fabrication steps and extreme scalability. We perform a detailed numerical study to evaluate the effects of channel doping concentration, dielectric constant of underlap spacers, source/drain resistance on logic performance of 20 nm gate length JL MOSFETs in terms of ON-current at a given OFF-current, subthreshold swing, gate capacitance and intrinsic delay for supply voltages ranging 0.4–0.75 V. In comparison with the reported experimental data for inversion-mode device, our optimized JL device exhibits enhancement of I_{ON} by 15.6%, reduction of drain-induced barrier lowering (DIBL) by 22.5% while preserving equally low SS of 61.5 mV/decade at channel length of 34 nm and supply voltage of 0.75 V.

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1. Introduction

Due to limited battery lifetime, the ultra-low power CMOS design at more advanced technology nodes has become the focus of research in industry and academia because of its myriad of applications such as cellular phones, healthcare, personal digital assistant and other portable computing devices [1–3]. However, in aggressively scaled devices the short channel effects (SCEs) that degrade subthreshold characteristics come into play. As a result the ultra-low power operation of such devices becomes deteriorated. The ultra-low power performance metrics of MOS devices may be identified as subthreshold slope (SS), ratio of ON-current (I_{ON}) to OFF-current (I_{OFF}) or I_{ON} for a given I_{OFF} , gate capacitance C_{gg} and delay [4,5]. It is well known that the use of multigate MOS structure reduces the SCEs considerably. In such structures SCEs are suppressed further using an ultra-thin silicon body and even further with the adoption of underlap gate-source/drain (S/D) together with a high-k spacer layer [6–8]. Among various high-k dielectrics, HfO_2 , ZrO_2 , Al_2O_3 , La_2O_3 , etc. may be used as sidewall spacer layers in nanoscale MOSFETs as they have pretty high dielectric constant, acceptable amount of conduction and valence band offsets with Si and also are thermodynamically stable with Si [9,10]. There have been many reports regarding the impact of various single high-k sidewall spacer layers on the logic and analog/RF performance of MOSFETs [5,8,11,12]. The source/drain resistance plays an important role in determining the characteristics of MOSFETs particularly at the nanodecameter technology

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nodes. There have been numerous findings in the literature, mostly on the formation of source/drain resistance of inversion mode transistors at different channel lengths [13–15]. In recent years transistors without a junction, also termed as junctionless transistors (JLTs), have become popular due to their remarkably simpler process technology, scalability and promising characteristics [16–20]. JLTs are able to leverage optimized channel doping concentration, underlap spacer length and dielectric constant, and reduced source/drain resistance to yield excellent ultra-low power logic performance. Although there have been some reports of JLTs on analog and logic circuit performance in the literature [21–24], a comprehensive study of JLTs for low power logic applications taking into account various device design parameters i. e., structural, material and electrical parameters is still lacking, however, particularly at the current technology node.

In this paper, we investigate the logic performance of JLTs at channel length of 20 nm highlighting the dependence of low-power performance metrics or figures of merit on different device design parameters such as channel doping concentration, spacer dielectric constant, and source/drain (S/D) resistance at various drain to source bias conditions in the range 0.4–0.75 V. Furthermore, our optimized values of performance metrics for JLTs exhibit improvement over the reported experimental data for inversion mode (IM) devices published elsewhere [3] at the same channel length and supply voltage of operation.

2. Device structure and simulation setup

In the present study we consider a double gate (DG) junctionless transistor having symmetrical underlap gate-source/drain at $L_g = 20$ nm, as shown in Fig. 1, with various device design parameters entered in Table 1. We use the numerical device simulator SILVACOATLAS [25] to simulate the DGJLT. To capture the carrier mobility the Lombardi CVT model is used. In order to include generation-recombination events properly Shockley-Read-Hall (SRH) and Auger recombination models are included. As in JLTs the channel doping concentration is usually high, the band gap narrowing model is invoked and the Fermi-Dirac carrier statistics is also activated. The drift-diffusion transport model is employed with adjusted carrier saturation velocity as recommended in Ref. [26]. In addition density gradient (DG) model, which is compatible with drift-diffusion approach, is enabled in order to include quantum potential correction in the current density expression as the gate length is below 30 nm. The quantum-mechanical effects are not significant in the subthreshold analysis of our devices as the thickness of the Si body is 5 nm [27].

3. Model calibration

The models used in the simulation setup were calibrated by comparing our simulated transfer characteristics with the experimental characteristics reported in Ref. [17] as shown in Fig. 2 using the same device structure and parameters at both high and low drain bias conditions. The fabricated silicon channel junctionless transistor in Refs. [17], with which we

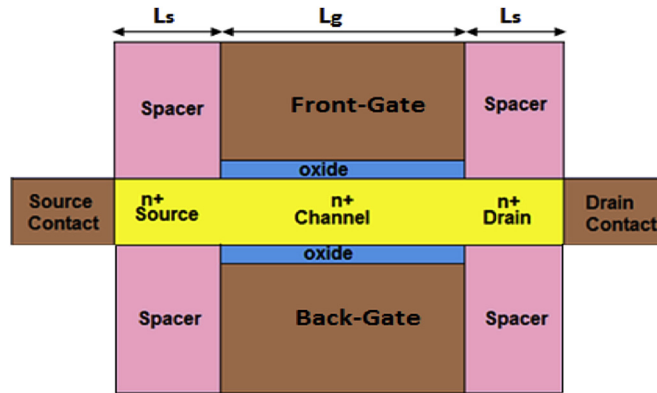


Fig. 1. Schematic diagram of a junctionless double gate MOSFET with underlap spacer layers. Various insulators with different dielectric constants in the range 1–30 are used as spacer layers. L_g and L_s denote the gate length and spacer length, respectively.

Table 1
Device parameters of JLTs used in simulation.

Sl. no.	Device parameters	Values
1.	Gate length	20 nm
2.	Silicon channel thickness	5 nm
3.	Width	1 μm
4.	Donor-type channel doping concentration	$5 \times 10^{18} - 3 \times 10^{19} \text{ cm}^{-3}$
5.	Equivalent gate oxide thickness (EOT)	1 nm
6.	Source/drain resistance	50–180 $\Omega\text{-}\mu\text{m}$

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