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Analytical model of LDMOS with a single step buried oxide layer

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ABSTRACT

In this paper, a two-dimensional analytical model is established for the Single-Step Buried Oxide SOI structure proposed by the authors. Based on the two-dimensional Poisson equation, the analytic expression of the surface electric field and potential distributions for the device is achieved. In the SBOSOI (Single-Step Buried Oxide Silicon On Insulator) structure, the buried oxide layer thickness changes stepwise along the drift region, and the electric field in the oxide layer also varies with the different buried oxide layer thickness. These variations will modulate the surface electric field distribution through the electric field modulation effects, which makes the surface electric field distribution more uniform. As a result, the breakdown voltage of the device is improved by 60% compared with the conventional SOI structure.

To verify the accuracy of the analytical model, the device simulation software ISE TCAD is utilized, the analytical values are in good agreement with the simulation results by the simulation software. The results verified the established two-dimensional analytical model for SBOSOI structure is valid, and it also illustrates the breakdown voltage enhancement by the electric field modulation effect sufficiently.

The established analytical models will provide the physical and mathematical basis for further analysis of the new power devices with the patterned buried oxide layer.

1. Introduction

As the SOI (Silicon On Insulator) structure is convenient for forming good electrical isolation with the buried oxide layer in the device, so it attracted more and more researchers working on it, and great progresses have been achieved for the HVIC (High Voltage IC) and SPIC (Smart Power IC) based on SOI devices in recent years [1–4].

For the designing of SOI power devices, breakdown voltage is a key parameter. The breakdown voltage of SOI structure is determined by the lower value between the lateral breakdown voltage and the vertical breakdown voltage of the device, so the optimization for both the lateral and vertical electric field is essential [5–10]. For the electric field distribution optimization, the author proposed several new structures: single step buried oxide layer SOI (SBOSOI) structure [11], double step buried oxide layer SOI (D-SBOSOI) structure [12], P-type buried layer SOI (BPSOI) structure [13], air partial SOI (APSOI)

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structure [14], folded silicon SOI structure [15]. With the electric field modulation effect, these transformations of buried oxide layer would introduce new electric field peaks into the surface, which makes the surface electric field distribution more uniform [16], and the performance of the SOI LDMOS is significantly increased.

However, these new structures do not have the detailed theoretical supports, and the electric field modulation effect in these devices have not been essentially explained. So, further investigation on these structures is necessary to provide scientific basis and guidance for designing and analyzing of such devices.

In this paper, based on the Single-Step Buried Oxide SOI structure (SBOSOI) proposed by the authors, the interactions of the lateral and vertical electric fields are taken into account, and the analytical models of the electric field and potential distributions for the device are achieved through solving the 2D Poisson equation. The influence of different device parameters on its performance is analyzed by the device simulation software ISE TCAD. The new electric field peak introduced by the step buried oxide layer is confirmed by the analytical model, which illustrates the influence of electric field modulation effect on the surface electric field distribution.

2. SBOSOI structure and model

A schematic cross section of the SBOSOI LDMOS is illustrated in Fig. 1. The SBOSOI LDMOS can be obtained through the conventional SOI LDMOS fabrication technology based on a wafer with single step buried oxide layer. The critical process steps can be described as follows:

First of all, the wafer with a single step buried oxide layer should be manufactured.

Firstly, as is shown in Fig. 2, the silicon wafer should be etched to form a steep step.

Secondly, a 0.02 μm thin oxide layer is grown by the dry-oxygen oxidation method, then the deposition method will be used to form a 1 μm oxide layer and the CMP technology is used to achieve the planarization of the oxide layer. The particularly manufactured wafer with a step oxide layer is shown in Fig. 3.

Thirdly, bonding the particularly manufactured wafer mentioned above with an ordinary wafer with a 0.5 μm oxide layer. And after thinning and CMP technology, the final wafer with a single step buried oxide layer will be achieved as is shown in Fig. 4.

After the wafer is manufactured, the conventional LDMOS fabrication technology can be used based on the new SOI wafer to achieve the proposed device. Fig. 5 is the SBOSOI LDMOS achieved through the process simulation.

2.1. The analytical model under complete depletion

Based on the step buried oxide layer thickness, the drift region is divided into two regions: region I and region II, the thickness of the buried oxide layer in region I and region II are t_{ox1} and t_{ox2} respectively, the length of the two regions are L_1 and (L_2-L_1) respectively. The doping concentration in the drift region is N_d, the drift region thickness is t_s. The voltage applied on the drain electrode is V_d. When the device is reverse biased and the drift region is fully depleted, the potential distribution in region I and region II is described by the following two-dimensional Poisson equation:

$$\frac{\partial^2\phi_i(x,y)}{\partial x^2}+\frac{\partial^2\phi_i(x,y)}{\partial y^2}=-\frac{qN_d}{\varepsilon_s},\ \mathrm{i}=\mathrm{I},\mathrm{II} \tag{1}$$

The boundary conditions are given by Ref. [2]~ [9]:

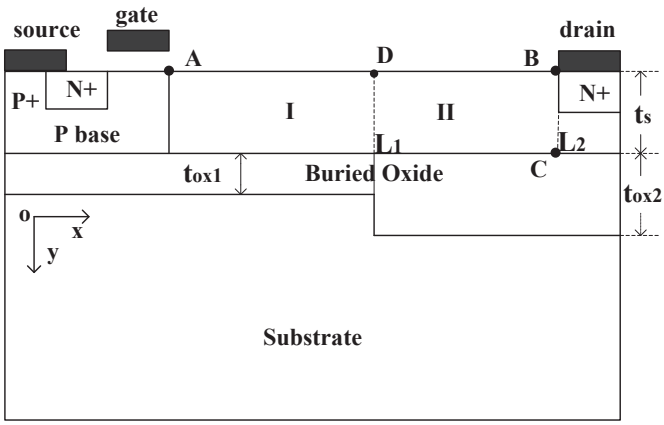

Fig. 1. Cross section of SBOSOI LDMOS structure.